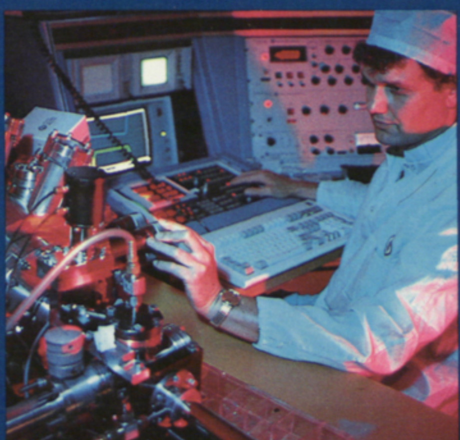
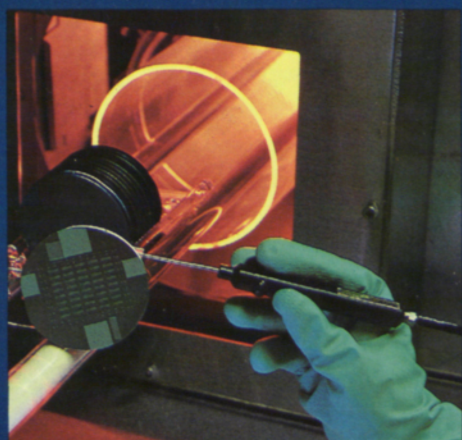
ENGINEERING

CORNELL QUARTERLY



VOLUME 22
NUMBER 3
SPRING 1988

NANOFABRICATION:
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IS BETTER


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IN THIS ISSUE

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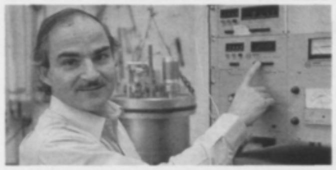

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Engineering: Cornell Quarterly (ISSN 0013-7871), Vol. 22, No. 3, Spring 1988. Published four times a year, in autumn, winter, spring, and summer, by the College of Engineering, Cornell University, Campus Road, Ithaca, New York 14853-2201. Second-class postage paid at Ithaca, New York, and additional offices. Subscription rates: $6.00 per year or $9.00 outside the United States.

Opposite: A scene in Knight Laboratory, home of the National Nanofabrication Facility on Cornell's engineering campus.

Outside cover, clockwise from upper left: Knight Laboratory; lithography with the JEOL system; ion implantation; a wafer being inserted into a high-temperature furnace; the scanning Auger microprobe.

TEN YEARS OLD AND GOING STRONG

A Commemoration of a Decade of Research at Cornell's National Nanofabrication Facility

by Edward D. Wolf

If Ezra Cornell could see what is going on today at his university, he would be pleased. His famous declaration that he "would found an institution where any person can find instruction in any study" was highly innovative in his day. Now, almost one hundred fifty years later, Cornell University is still in the vanguard. In new ways, with new resources, it continues to meet the educational needs of the times.

Cross-disciplinary research and education thrive at Cornell today in a modern expression of the university's traditional diversity. There are several good reasons for this. One is that the Graduate School is organized into fields of study whose boundaries transcend those of departments and colleges. Another is the presence of strong interdisciplinary centers and programs: Cornell is home to six national research centers, along with nearly twenty local centers and programs. The result is a dynamic, stimulating environment conducive to the development of ideas and new perspectives and attractive to top-notch students and faculty members.

The National Nanofabrication Facility (NNF) is a prime example. It is unique among university research centers: it is the only one that provides the complete resources for fabricating structures with dimensions in the micrometer and nanometer regime, and it is open to researchers throughout the country.

BRINGING PEOPLE AND TECHNOLOGY TOGETHER

At the NNF, students, faculty members, scientists, and engineers from universities, industry, and national laboratories work together to apply nanofabrication techniques to innovative research projects in more than fourteen disciplines. Current programs run the gamut from research on how a fungus infects a bean plant to the development of gratings for the study of distant galaxies. Of course, there are programs in all aspects of microelectronics: examples are magnetic bubble logic, high-electron-mobility transistors, 0.25-micrometer CMOS devices, and integrated optoelectronics.

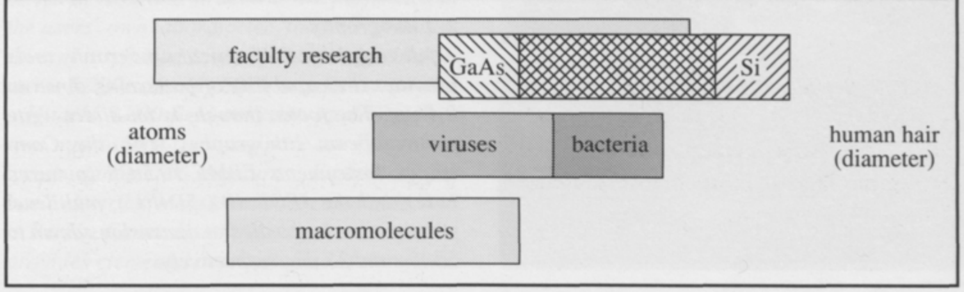
But although innovative research and

Below: The chief administrators of the NNF are Edward D. Wolf, director (at right), and Gregory Galvin, deputy director.

DIMENSIONAL RANGES

One micrometer (µm) = 10^{-6} meter; one nanometer (nm) = 10^{-9} meter; one angstrom (Å) = 10^{-10} meter

	Sub-nanometer structures	Nanometer structures		Sub-micrometer structures	Micrometer structures	
µm	.001	.01	.1	1	10	100
nm	1	10	100	1,000		
Å	10	100	1,000	10,000		



The chart shows the lateral (two-dimensional) size domain of nanostructures. Equally and often more important is the control of the vertical (thickness) dimension, which can range from a few Å to near 1 µm.

state-of-the-art technology attract much attention, the basic reason for the NNF—its real contribution to the future—is what it can offer to students. Each year more than forty graduate degrees are awarded to students who have used the NNF. At any time there are, all told, more than two hundred fifty students who are authorized users of the facility. And by users, we mean hands-on, in-the-laboratory users. With staff help, a student is free to use equipment whose price may be millions of dollars, whenever it is available, twenty-four hours a day. There is no better way to educate people in these advanced technologies.

AN EXPERIMENT THAT HAS PAID OFF

The NNF began in 1977 as an experiment by the National Science Foundation and Cornell University to discover how the technology of microfabrication—which requires very expensive equipment and maintenance—could be made available to the broad community of researchers at universities, in industry, and in federal laboratories who had need of that technology to pursue their programs. The center was first called the National Research and Resource Facility for Submicron Structures (NRRFSS)—the original emphasis was on structures whose minimum dimensions were typically between 0.25 µm and 1.0 µm (1 micrometer = 10^{-6} meter).

The response to this new center was tremendous, and in only a few years a new methodology for conducting advanced

"It is unique among university research centers. . . ."

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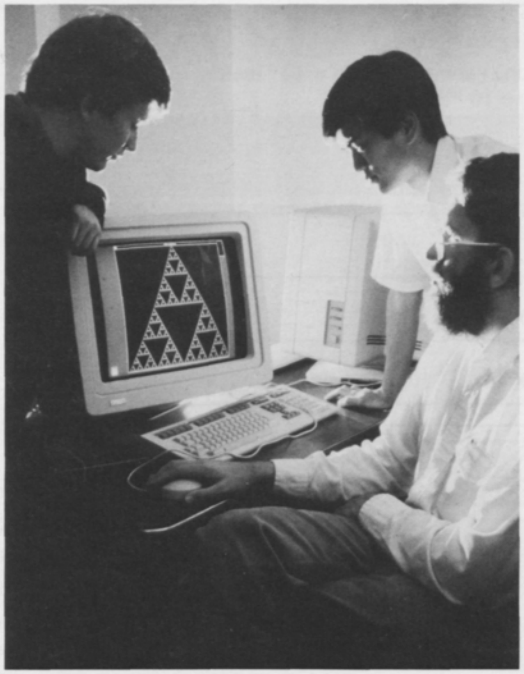

Major equipment at the NNF, including the instruments shown in the photographs on these pages, provides facilities for design, lithography, pattern transfer, and inspection.

1. Design
A network of computer systems is used for a variety of operations from device modeling to data collection. The central system is a Digital Equipment Corporation VAX 8530; clustered with it are five VAXstation-II/GPX color-graphics workstations (such as the one pictured here) used for computer-aided design.

2. Lithography
A full complement of optical lithography tools provides the capability of patterning down to 0.4 μm. The focus, though, is on direct-write electron-beam lithography. With the Cambridge Instruments EBMF-10.5/CS (pictured here) and the JEOL JBX-5DII(U), multilevel patterns can be created at dimensions down to 50 nm and 25 nm, respectively.

2

research in the university environment had been established. In recent years this methodology has become the norm for federally supported engineering research centers at universities throughout the United States.

Students and faculty members from Cornell and other universities, engineers from industrial concerns, and scientists from federal laboratories soon filled NRRFSS to capacity. American industry was quick to become a partner in the enterprise, too. Before long, industrial support through grants, discounts, and donations accounted for half the annual budget of the facility.

One of the major users of the NNF is the Semiconductor Research Corporation (SRC), a cooperative organization of leading United States semiconductor, computer, and telecommunication industries. Cornell is one of the first "centers of excellence" established by the SRC for research

3. Pattern Transfer
A wide range of instruments is available for both additive and subtractive pattern transfer. Techniques include thin-film deposition by evaporation or sputtering; ion implantation with ion energies from 5 keV to 600 keV; and reactive-ion etching with either fluorine-based or chlorine-based chemistry, used for dry processing of high-aspect-ratio structures. This Genus chemical-vapor deposition system provides the capability for selective deposition of tungsten.

4. Inspection
Although most of the measurements of completed devices and structures are performed in the users' own laboratories, the NNF provides several inspection tools. A Cambridge Instruments S-200 scanning electron microscope and a Hitachi S-800 field-emission scanning electron microscope (pictured) are used to photograph nanometer structures. Equipment for basic electrical measurements is available, and a Perkin Elmer scanning Auger microprobe provides elemental depth profiles of thin films.

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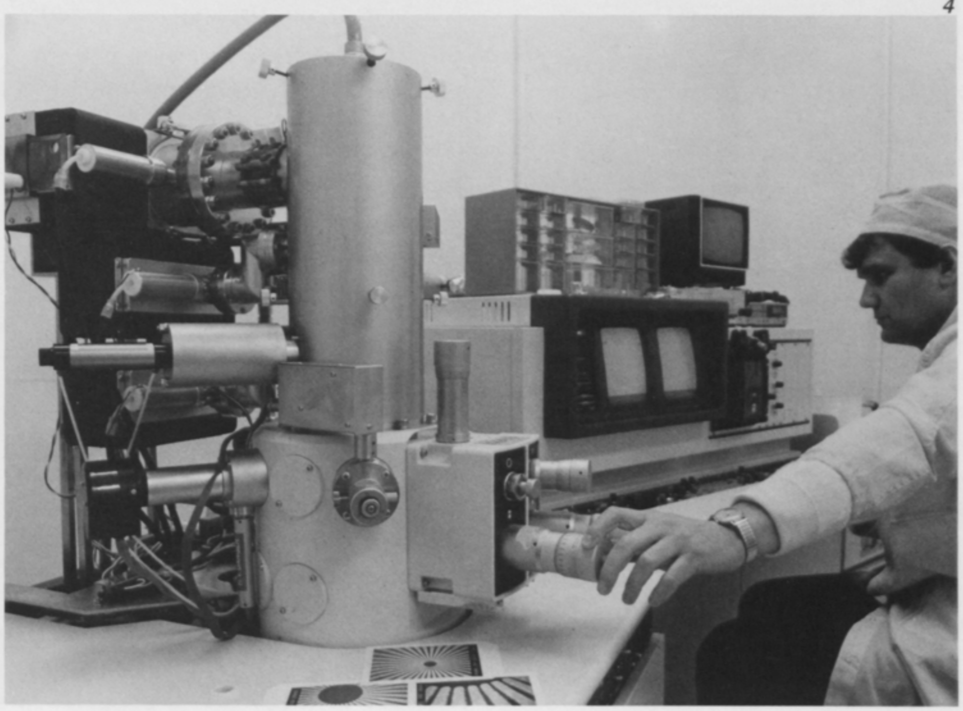


on VLSI (very large scale integrated) circuits. The SRC Program on Microscience and Technology at Cornell was organized to promote an expansion of the knowledge base in these fields, to provide for the training of new researchers, and to foster interaction among industrial and academic researchers. More than twenty faculty members from four departments, and some forty graduate students, currently participate in the program, which is funded at about $1.4 million a year. The director is Noel C. MacDonald, professor of electrical engineering.

A GREATER MISSION BASED ON SHRINKING DIMENSIONS

In 1987 the NRRFSS was succeeded by the NNF, in recognition that the lower limits of structural dimension were dropping. While the NNF continues the policies and success of its predecessor, it has a bold new

Who Are the Users of the NNF?

Cornell University

Of the one hundred six projects listed as current by the National Nanofabrication Facility, over half (fifty-eight) are being carried out by Cornell researchers. Seven academic units are represented, sometimes with several projects headed by the same faculty researcher. The schools or departments and the professors who are heading these current projects are:

School of Applied and Engineering Physics (seven projects): Robert A. Buhrman, Michael Isaacson, Aaron Lewis, John Silcox, Watt W. Webb

School of Chemical Engineering (one project): Ferdinand Rodriguez

Department of Chemistry (two projects): Héctor D. Abruña, George H. Morrison

School of Electrical Engineering (twenty-five projects): Lester F. Eastman, Peter Krusius, Charles A. Lee, Noel C. MacDonald, Chung L. Tang, George J. Wolga, S. Simon Wong, Edward D. Wolf

Department of Materials Science and Engineering (fifteen projects): Dieter G. Ast, James M. Blakely, Barry Carter, Herbert H. Johnson, Edward J. Kramer, Che-Yu Li, James W. Mayer, Arthur L. Ruoff, Stephen L. Sass, Michael O. Thompson

Department of Physics (seven projects): Jeevak Parpia, Robert Pohl, Robert Thorne, Robert Richardson, Robert Silsbee

Department of Plant Pathology (one project): Harvey C. Hoch

Other Universities

University of Arizona: Optical Sciences Center (two projects)

California Institute of Technology: Department of Applied Physics

University of California at San Diego: Department of Physics (two projects)

Carnegie-Mellon University: Department of Electrical and Computer Engineering (three projects)

University of Cincinnati: Department of Electrical and Computer Engineering

Clarkson College of Technology: Department of Electrical and Computer Engineering

University of Colorado: Department of Electrical and Computer Engineering (three projects)

Indiana University: Department of Chemistry

Ohio State University: Department of Electrical Engineering; Department of Physics (two projects)

University of Minnesota: Department of Physics and Astronomy

State University of New York at Buffalo: Department of Physics and Astronomy

University of Pennsylvania: Department of Materials Science and Engineering; Department of Orthopaedic Surgery Research; Department of Physics

University of Rochester: Department of Mechanical Engineering

University of Rochester Medical Center: Department of Biophysics (two projects)

University of Virginia: Department of Electrical Engineering (three projects); Department of Physics

Yale University: Section of Applied Physics

National Laboratories

Jet Propulsion Laboratory

Marine Biological Laboratory

National Bureau of Standards, Microelectronics Dimensional Metrology

National Institutes of Health, Laboratory of Neurophysiology

Naval Research Laboratory, Microwave Technology Branch

Sandia National Laboratories

Industrial Organizations

BDM Corporation, Physical Sciences Technology

Bell Communications Research

General Electric Company, Electronics Laboratory

GTE Laboratories

IIT Research Institute

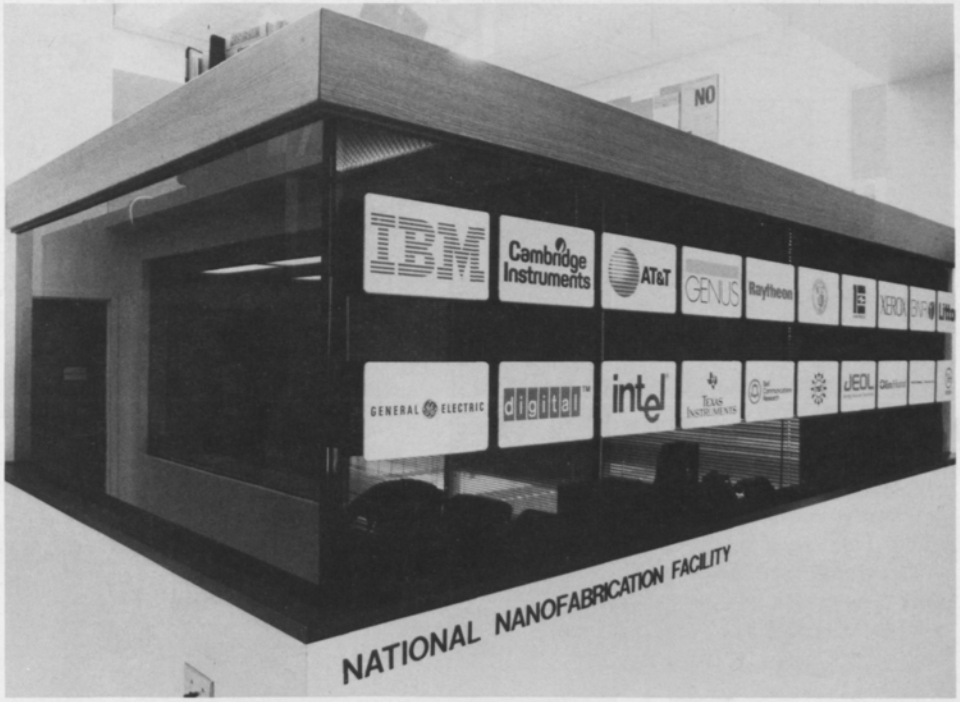
LTV Aerospace and Defense Corporation, Missiles and Electronics Group

McDonnell Douglas Astronautics Company, OptoElectronics Center (two projects)

Motorola, Inc., Compound Semiconductor Laboratory (two projects)

Siemens Research Laboratories

United Technologies Research Center, Microelectronics Department



Left: Corporate insignia on display in the reception area of the NNF suggest the nature of the facility: a resource for researchers from industry, as well as from government and university laboratories.

mission: fabricating structures at dimensions from 25 nm to 100 nm (1 nanometer = 10^{-9} meter). Structures in this range are fully ten times smaller than those the NRRFSS focused on.

The NNF can be viewed more broadly as having the role of a facilitator of high-technology research. It provides the infrastructure that makes such research possible at a university; equipment, staff expertise, and program management are made available. And as an established, highly visible center, the NNF provides the impetus for new programs, support for fledgling projects, the mechanism for garnering matching support, and a focal point that brings together multiple, diverse disciplines that otherwise might not meet. This new methodology for research is an excellent example of the symbiotic relationship between the needs of an individual principal investigator and those of a directed, cross-disciplinary program. It is an arrangement in which the resulting accomplishments are truly greater than the sum of the parts.

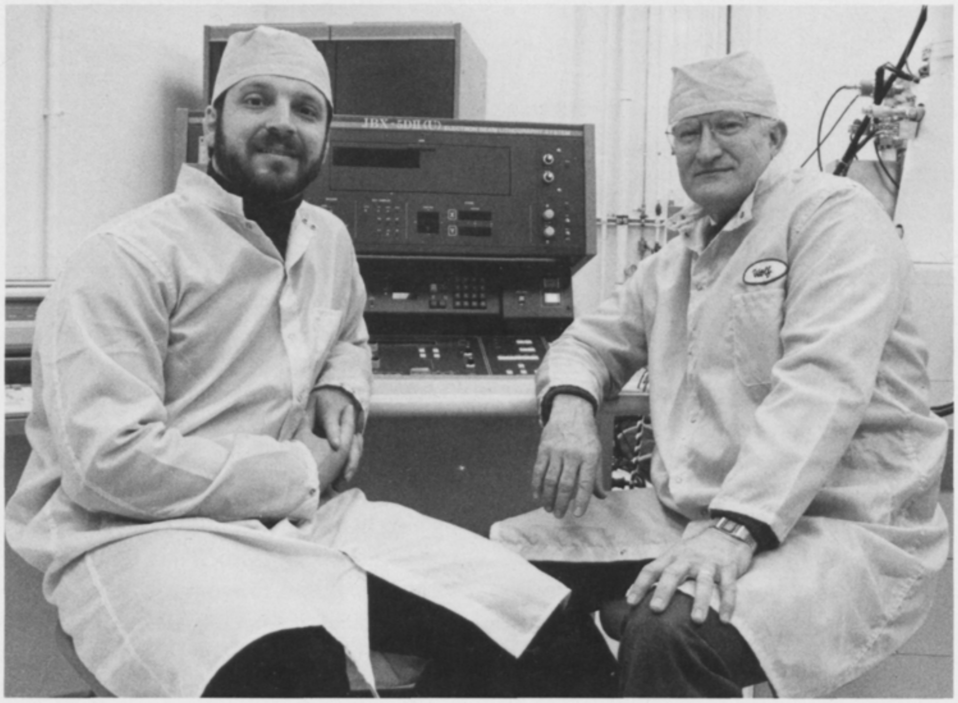
Hands-on use of the equipment; the bringing together of many diverse disciplines in one laboratory; partnership between university and industry for technology exchange; frequent interaction among researchers from Cornell and from laboratories throughout the country; the opportunity for faculty, students, and staff to work together in pursuit of common goals: these are the features that make the NNF so special. What better way could there be to promote the education of scientists and engineers who are well equipped to meet the technical and organizational challenges of modern research?

As a nation we currently face challenges in research, in education, in economic competitiveness, and in international leadership. Yet we also have before us a future of unprecedented opportunity. The NNF and similar centers are helping to shape that future through research at the forefronts of emerging technologies and through education of tomorrow's leaders.

This issue of *Engineering: Cornell Quarterly* commemorates the first decade of research at the National Nanofabrication Facility and provides a hint as to what lies in store during the coming decade. The following articles by Cornell researchers—a small sampling of the work in progress—provide a glimpse into the exciting world of the very small.

FABRICATING TRANSISTORS IN THE NANOMETER DOMAIN

by Richard C. Tiberio and Edward D. Wolf



Above: NNF staff member Richard C. Tiberio (on the left) and Edward D. Wolf, the director of the facility, are shown with the JEOL scanning electron-beam lithography system used to fabricate patterns with dimensions in the nanometer range.

The continued growth of the microelectronics industry has been fueled in large part by the ability to fabricate smaller and smaller electronic devices. In recent years, the technology available to us for device fabrication has evolved to a level that now allows us to enter the nanometer domain. Here the critical dimensions are measured in nanometers—billionths of a meter—and new physical phenomena, not observed in prior devices of larger dimensions, come into play. Building useful electronic devices in this environment will require new insights, knowledge, and techniques.

One of the foremost practical applications of nanometer electronics is to high-speed electronic devices for use at millimeter-wave and microwave frequencies. Research on these devices, such as our group at Cornell is conducting, will also lead to new insights about the physics taking place in the nanometer (nm) domain, particularly as we drop below 100 nm.

Our work has been focused on developing new lithographic techniques for field-effect transistors (FETs) based on compound-semiconductor materials such as gallium arsenide and aluminum gallium arsenide. The critical dimension in devices of this type is that of the gate—the structure that controls current flow. In addition to controlling the length of the gate at sub-100-nm dimensions, we must very accurately position the gate between the source and the drain of the transistor.

The first such devices we fabricated were MESFETs (metal-semiconductor field-effect transistors). More recently, we have worked with a new class of high-performance devices, the HEMTs (high-electron-mobility transistors). Devices of this new kind are also discussed in this issue by Paul J. Tasker and Lester F. Eastman, who use the term MODFET (modulation-doped field-effect transistor).

NEW INSTRUMENTS PROVIDE NEW RESEARCH OPPORTUNITIES

The National Nanofabrication Facility (NNF) at Cornell spent several years raising the funds to purchase one of the most advanced scanning electron-beam lithography systems that is commercially available, the JEOL JBX-5DII(U). That system was made operational a little over a year ago. One of our first tasks was to characterize its performance so that it could be used to fabricate a variety of research devices with nanometer dimensions.

A critical measure of the performance of an electron-beam lithography system is its alignment accuracy—that is, the ability of the system to write the second level of a pattern so that it lines up perfectly with the previously exposed first level. To assess the alignment accuracy of the new JEOL system, we created a vernier pattern with a resolution of 5 nm, one of the highest resolution verniers ever fabricated. An electron micrograph of the pattern is shown in Figure 1. The average alignment accuracy exhibited by the system was better than ±20 nm, which is the best accuracy ever achieved with this type of instrument.

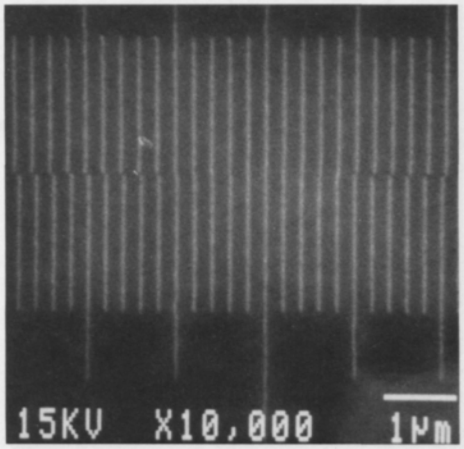


Figure 1. A scanning electron microscope (SEM) photograph of the vernier pattern created at the NNF. Note especially how well the central line of the upper part of the pattern (the first exposure) is aligned with the central line of the lower part (the second exposure): this indicates a shift of less than 5 nm.

The JEOL system has brought to our research the capability of fabricating patterns at dimensions well into the nanometer domain. We have produced metal lines as narrow as 25 nm using a polymer coating of poly(methyl methacrylate).

APPLYING THE RESULTS TO ACTUAL DEVICES

Research on fabrication processes has stimulated collaboration with industrial partners as well as with Cornell colleagues.

"Building useful electronic devices in this environment will require new insights, knowledge, and techniques."

Two recent papers demonstrate the collaborative nature of our research. At the International Symposium on Electron, Ion and Photon Beams, held in Los Angeles last June, we and some of our collaborators presented a paper on the fabrication of 100-nm-gate gallium arsenide MESFETs that had some of the best performance properties ever reported.[1] A joint paper with researchers at General Electric in Syracuse discusses the fabrication and performance of 100-nm-gate HEMTs that have the best gain and noise characteristics reported to date.[2] Figure 2 shows the nanotopography of one of these advanced HEMT devices.

The results of our research in this area demonstrate the utility of multilevel electron-beam lithography for fabricating devices and studying structures in the nanometer domain. The next step is to extend the fabrication processes to even smaller dimensions, below 100 nm. This should put us in the realm where new device concepts and material behavior can be explored. Numerous research opportunities exist at these small dimensions and we are proud to be part of a Cornell team that is at the forefront of nanometer science and technology.

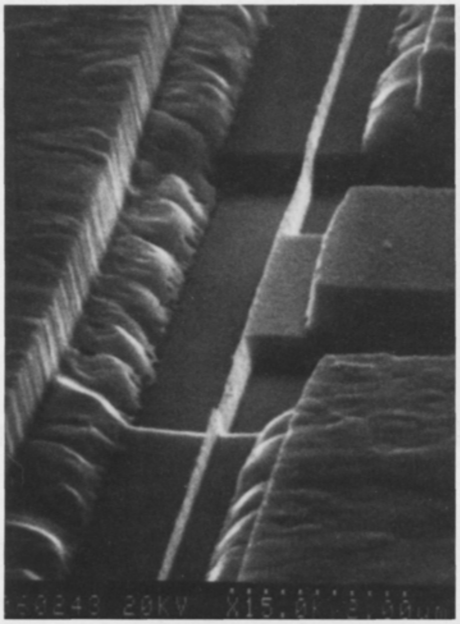


Figure 2. A scanning electron micrograph of a HEMT with a gate length of 100 nanometers. The thin wall at center is the gate. The source is on the right and the drain on the left.

[1]Tiberio, R. C., E. D. Wolf, S. F. Anderson, W. J. Schaff, P. J. Tasker, and L. F. Eastman. 1988. Fabrication and characterization of ultrashort gate length GaAs field-effect transistors.

[2]Chao, P. C., R. C. Tiberio, K.-H. G. Duh, P. M. Smith, J. M. Ballingall, L. F. Lester, B. R. Lee, A. Jabra, and G. G. Gifford. 1987. 0.1-μm gate-length pseudomorphic HEMT's. *IEEE Electron Device Letters* EDL-8(10).

Richard E. Tiberio is a staff member of the NNF and also a graduate student in electrical engineering. Edward D. Wolf is a professor of electrical engineering at Cornell and director of the National Nanofabrication Facility.

Tiberio already holds two Cornell degrees —the B.S. (1976) and the M.Eng. (1977). While an undergraduate, he served as a research assistant at Cornell's Laboratory of Atomic and Solid State Physics, and as an M.Eng. candidate he worked in the microelectronics and microwave laboratory. After two years at IBM, working with electron-beam systems, he became a system manager at the NNF. He has been a graduate research associate since 1986.

Wolf came to Cornell in 1978 from the Hughes Research Laboratories, where he simultaneously held the positions of senior scientist and section head in the Electron Device Physics Department. A graduate of McPherson College, he earned a doctorate at Iowa State University and was a postdoctoral researcher at Princeton University. He spent fifteen years in industrial research, first at the Rockwell International Science Center, and then at Hughes. Last year he spent a sabbatical leave as a visiting professor at Cambridge University, England. Wolf is a fellow of the Institute of Electrical and Electronics Engineers. He serves on a number of national technical committees and review boards.

LINKS TO THE OUTSIDE WORLD
in Submicron-Sized Silicon Devices

by James R. Phillips and James W. Mayer

Although transistors and other active devices in silicon form the heart of integrated circuits, it is the metal lines on silicon that form the connections to the outside world. As devices shrink to dimensions below micron sizes, the stability and integrity of these metal lines become important.

In research performed at the National Nanofabrication Facility (NNF) at Cornell, we have found that in some cases these structures are remarkably unstable. As a first step in finding a way to ensure stability, we have studied the reaction process, and we believe we know which mechanisms may be playing important roles.

Figure 1

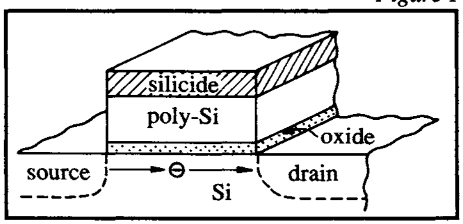
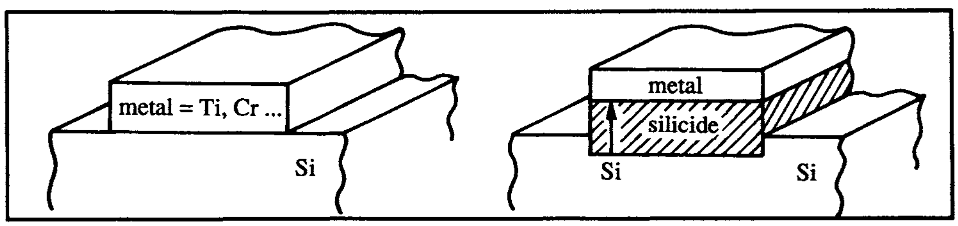


Figure 1. A field-effect transistor with a poly-Si gate and a silicide interconnect.

Figure 2. The formation of a silicide layer. At left: a titanium or chromium line on single-crystal silicon. At right: the subsequent formation of $TiSi_2$ or $CrSi_2$ and growth by transport of silicon through the silicide layer.

Figure 2



FINE-LINE SILICIDES IN FIELD-EFFECT TRANSISTORS

In a field-effect transistor, the control electrode, or gate, is often made of low-resistivity polycrystalline silicon (poly-Si), with a top connection of a metal-silicon compound, a silicide (Figure 1).

For our investigation, we used the NNF facilities to prepare fine-line silicides on poly-Si. We submitted the structures to various test conditions and examined them with a scanning electron microscope. What we discovered is that at process temperatures well below any melting temperature, the poly-Si dissolves in the silicide and then regrows as large silicon crystallites. The solid silicide layer acts as a growth medium for the dissolution, transportation, and subsequent growth of crystallites.

The rapid diffusion of silicon in silicides around 500° Celsius—which is less than one-half the melting point of silicon—is, in fact, the basis for the formation of the silicide layer during processing. Figure 2 illustrates a metal line of titanium or chromium deposited on silicon and subsequently heated to around 500°C. In the reaction between metal and silicon, the disilicide is formed at the interface. Silicon diffuses through the silicide layer and reacts with the metal until all the metal is consumed.

Such silicide structures are usually quite stable on single-crystal silicon substrates, even when they are processed at relatively high temperatures. With poly-Si, however, the same stability is not found, especially when the grain size is very small. (The grain size we worked with is about 30 nanometers or trillionths of a meter.)

"As devices shrink to dimensions below micron sizes, the stability and integrity of these metal lines become important."

Figure 3

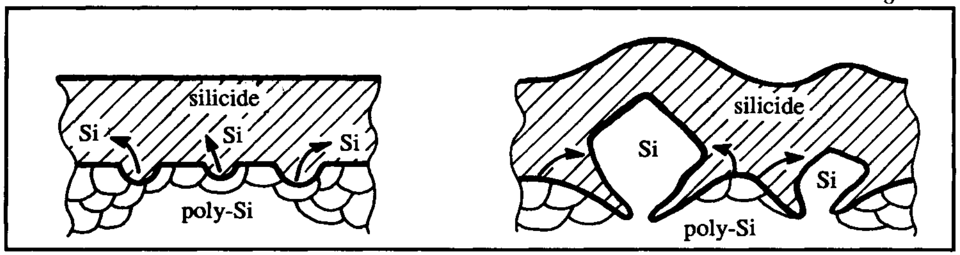


Figure 3. The effect of heat treatment on a silicide layer over fine-grained poly-Si. Left: Silicon dissolves and diffuses into the silicide. Right: Nucleation and growth of silicon crystallites requires deformation of the silicide layer.

DEFORMATION OF SILICIDE: THE INSTABILITY MECHANISM

In polycrystalline films, large grains grow at the expense of small grains if there is sufficient atomic mobility. In silicide/poly-Si structures, fast silicon transport in the silicide provides this mobility, as illustrated schematically in Figure 3. In order to accommodate the growing silicon crystallites, the silicide layer must deform.

The transformation of fine-grained poly-Si to large grains of silicon embedded in the silicide is illustrated in Figure 4. Included in the figure are cross-sectional transmission electron micrographs of a section of a titanium disilicide sample before and after heat treatment, clearly showing the growth of the large crystals, nearly a micron long, and the accompanying deformation of the silicide.

We have investigated the growth of silicon crystallites in a number of refractory-metal silicides. Invariably, the growth temperature is substantially higher than the silicide-formation temperature, which is generally considered to be the temperature at which silicon has a high atomic mobility in these silicides. Consequently, there must be another mechanism acting to limit the growth of the crystallites. We believe that crystallite growth depends on deformation of the growth medium—the silicide. The deformation of silicides is sensitive to temperature; they exhibit extensive softening at elevated temperatures that are close to 0.6 of the melting temperature, T_M. Since these temperatures, 0.6 T_M, correlate roughly with those at which crystallite growth occurs, the implication is that deformation plays a role in crystallite growth.

OBSERVING SILICIDE DEFORMATION IN FILMS

One would expect that the deformation would be different at the edges of the silicide film than it is in the central portions. To see if this is so, we again used the facilities at the NNF. We fabricated silicide lines of various widths on fine-grained poly-Si layers, heat-treated the structures at 900°C, and examined them with the scanning electron microscope before and after the silicide layer was etched away.

The micrograph in the upper part of Figure 5 shows a view of $CrSi_2$ on poly-Si after the heat treatment. The silicide line is bowed and there are hillocks and protrusions at the line edges. The lower micrograph in Figure 5, taken after the silicide layer had been etched away, reveals the hillocks as large silicon crystallites. The poly-Si in the center of the line is missing: it is this poly-Si that is the source of silicon

Figure 4

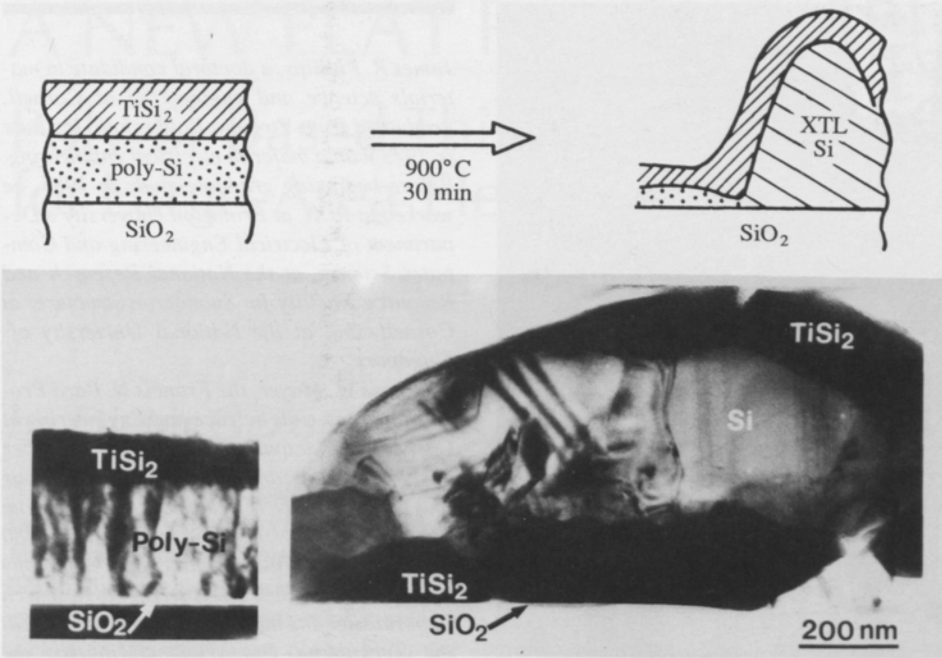


Figure 5

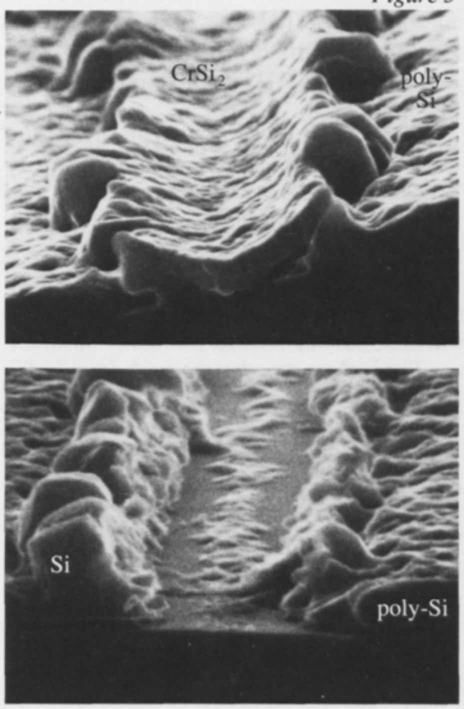


Figure 6

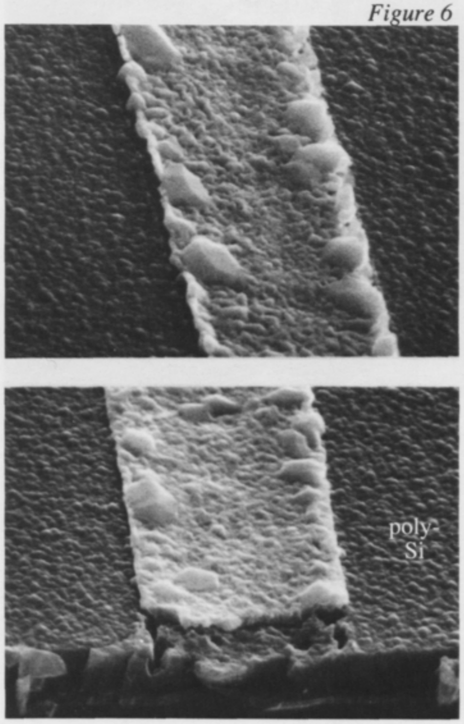


Figure 4. A sketch and cross-sectional TEM micrograph of a $TiSi_2$ layer on fine-grain poly-Si before and after annealing at 900°C.

Figure 5. SEM micrographs showing what happened when poly-Si with a line (about 1 μm wide) of $CrSi_2$ on top was annealed at 900°C. Above: the silicide is bowed and hillocks have formed. Below: with $CrSi_2$ removed, the hillocks are revealed as large silicon crystallites, and poly-Si is gone from the central line region.

Figure 6. Fine-line $CrSi_2$ on poly-Si after treatment at 700°C for 10 hours (above) and at 760°C for 90 minutes (below). Hillock formation and erosion of the poly-Si are shown to occur initially at the edges of the film.

for the growth of large crystallites at the edges of the film. Evidently the poly-Si dissolves in the silicide and then the silicon diffuses to the edges of the silicide line, where less silicide deformation is required for crystallite growth.

With these fine-line structures, deformation of the silicide occurs at lower temperatures—about 200°C lower—than in large-area structures. For example, in Figure 6 the upper micrograph shows that hillock growth is well developed at 700°C (well below 0.6 T_M) with crystallites as large as 0.5 micron across. The lower mi-

crograph, taken after an anneal at 760ºC and subsequent removal of a small segment of the silicide line, shows that erosion of poly-Si has taken place simultaneously with the growth of the silicon hillocks, leaving voids underneath the line edges.

In our current work we are trying to measure the energy barrier to the hillock growth. Knowing this would provide an important clue about which reaction mechanism—diffusion or deformation, for example—controls the rate of hillock growth. Understanding what mechanism is dominant should enable us to focus on the best ways to make the silicide lines stable.

James R. Phillips, a doctoral candidate in materials science and engineering at Cornell, graduated from Virginia Polytechnic Institute in 1973 with a major in electrical engineering. Before beginning graduate study in 1985, he worked at RCA, at Princeton University's Department of Electrical Engineering and Computer Science, at the National Research and Resource Facility for Submicron Structures at Cornell, and at the National University of Singapore.

James W. Mayer, the Francis N. Bard Professor of Materials Science and Engineering at Cornell, is principal investigator for a number of sponsored research projects, including four that make use of NNF resources. A Ph.D. from Purdue University, he came to Cornell in 1980 from the California Institute of Technology faculty. He has also worked at Hughes Research Laboratories and has been a visiting scientist at the Technische Hochschule (Munich), the Chalk River Nuclear Laboratories (Ontario), the Institute of Physics of the University of Modena (Italy), the Research Institute for Physics (Stockholm), and the University of Catania (Italy).

Mayer has received the Von Hippel Award of the Materials Research Society and the Silver Medal of the University of Catania. He is a fellow of the American Physical Society and the Institute of Electrical and Electronics Engineers, a scientific member of the Bohmische Physical Society, and a member of the National Academy of Engineering.

The authors note that the work described in this article was carried out with the collaboration of colleagues in the Department of Materials Science and Engineering: Les Allen, Liang-Sun Hung, Peter Revesz, and Long-ru Zheng. At the NNF, Bob Soave deposited the poly-Si films, Mike Skvarla carried out ion implantation, and Brian Whitehead assisted with electron-beam lithography. The work was supported in part by Intel Corporation and by the Program on Microscience and Technology, which is supported by the Semiconductor Research Corporation.

A NEW FLAT PANEL DISPLAY

Poly-Si-Based Thin-Film Transistors for Large-Area Electronics

by Dieter G. Ast

Almost all electronic devices today are fabricated on single-crystal silicon wafers—slices of single crystals grown from liquid silicon at high temperature. The largest crystals grown commercially are six inches in diameter, not big enough for many applications. While some large structures, such as solar cells, can be stitched together in arrays of single-crystal silicon wafers, others, including large-area sensors and printing heads, and screens for TVs and computers, cannot tolerate the "dead" areas along the joints. Large-area electronic devices such as image sensors or display panels require new building materials.

To be suitable for large-area devices, a material must not only meet the specific electronic requirements, but must be capable of being laid down in a thin film. Examples are amorphous selenium arsenide, which is coated onto the image-receiving drums of Xerox machines; and amorphous hydrogenated silicon, used to make solar cells, image sensors in TV pick-up tubes and copy machines, and thin-film transistors (TFTs) for large displays.

But the material in which my group at Cornell is particularly interested is polycrystalline silicon (poly-Si), which is already used in the construction of integrated-circuit elements such as gates and emitters and for fabricating TFTs. We are developing poly-Si-based TFTs with electronic properties suitable for the construction of large flat panel displays of the guest-host liquid-crystal type.

SEEKING AN ALTERNATIVE FOR VACUUM TUBES

The potential for a large commercial market has made display technology one of the most innovative, active, and interesting areas in electronics, although not much about the research appears in the journals. Talented people in many companies—manufacturers of consumer electronic products, computers, devices for avionics, and even automobiles—are working on the development of flat panel displays. The object is to displace the ubiquitous cathode-ray tube, the last holdout of vacuum-tube technology in consumer-information electronics. The feeling is widespread that its days are numbered.

In flat-panel-display technology, the main device is the *liquid-crystal display* (LCD). Liquid crystals are long, stiff, rod-like molecules that tend to arrange themselves parallel to their neighbors. Exposed to an electric field, they line up parallel to the field lines. Since their alignment can be directed, and since they are optically active crystals, they are convenient building blocks for displays. Furthermore, they consume very little power and can operate in reflection, which makes them readable in sunlight. Essentially, the LCD element, or pixel, is a small capacitor with the liquid crystal as the dielectric.

The best known type is the *twisted-nematic* (TN) display, which appeared first in digital watches and then spread to portable computers and TVs. Its next application will be to displace cathode-ray tubes in avionic devices. From a systems point of view, the most valuable characteristic of the TN display is its strongly nonlinear optical output. As Figure 1 shows, contrast develops only above a critical threshold of applied voltage, and then increases steeply.

MULTIPLEX ADDRESSING OF LIQUD-CRYSTAL DISPLAYS

The nonlinear, nearly "on-off" behavior shown in Figure 1 permits "line-at-a-time addressing", which dramatically reduces

Figure 1

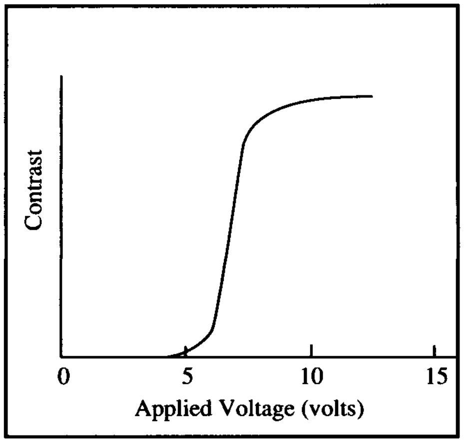


Figure 1. The strongly nonlinear optical output characteristic of the TN liquid-crystal display, the kind used in digital watches. The voltage has to exceed a critical threshold before contrast develops, but past the threshold, the contrast increases steeply. This nonlinear, nearly "on-off" behavior permits limited "line-at-a-time" addressing.

Figure 2

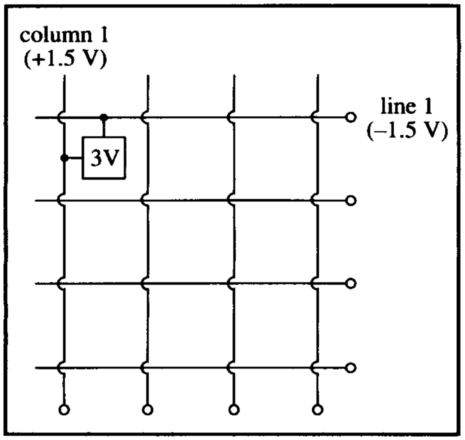


Figure 2. A simplified example of consecutive-line addressing.

To see how this works, assume that the minimum voltage required to generate contrast is 2 volts, and that we want to display information consecutively, starting at the first line. We set this line at −1.5 volts—insufficient to turn on any pixels. Pixels to be activated are addressed by setting their column leads to +1.5 volts—too low to activate pixels anywhere outside line 1. The crossover points along line 1 are activated, however, because the voltage differential is 3 volts. Once the selected liquid crystals have been aligned, a characteristic relaxation time must elapse before they can realign to the field-free state after the field is switched off. This allows us to proceed to the next line to repeat the cycle. Averaged over time, the liquid crystals respond to the root-mean-square average of the applied voltage. This effect limits the size of the display that is addressable with this technique.

the connections needed between the display and the driver electronics. A conventional TV has an effective resolution of about 350 lines, so to implement a comparable digital black-and-white display, we would need 122,500 individually addressable picture elements arranged into 350 rows and 350 columns. Color triples the number of elements required, since each black-and-white pixel is replaced by a red, a blue, and a green pixel. Using individual addressing, we would have to run 367,000 leads between the display and the drive electronics—clearly not feasible. With consecutive line addressing we would need only 525 connections along the four edges of the display—a number easily handled with current technology.

This addressing scheme is depicted in Figure 2. Unfortunately, there is a limitation. Although the scheme requires relatively high instantaneous voltages, the highest voltage that can be applied is set by the requirement that the root-mean-square average voltage of nonselected pixels anywhere in the display must stay below the threshold. Suppose, for example, we have a 200-line display (corresponding to 25 lines displayed on a computer screen); the maximum average voltage that can be applied to a selected pixel is only 8 percent higher than the threshold. Since contrast curves do not rise perpendicularly above the threshold, contrast inevitably diminishes as the number of lines increases.

Those of us who have experience with portable computers with LCD screens know that this loss of contrast goes hand-in-hand with a loss of viewing angle. Even the most expensive ("Supertwist") displays exhibit contrast and viewing angle far inferior to that found in a $2.98 watch.

Much better contrast and much larger viewing angle are possible with displays of the type known as *guest-host* (GH). These are used for avionics displays, which require high white-on-black contrast under full sunlight, and high contrast in the backlit mode for night viewing. The contrast-voltage curve of these displays rises so gradually that they cannot be multiplexed in the way described in Figure 2. Rather, they need individual control over each pixel element. This control is provided by separate high-voltage integrated circuits to which the display segments are wired up using a ceramic-chip carrier.

Figure 3

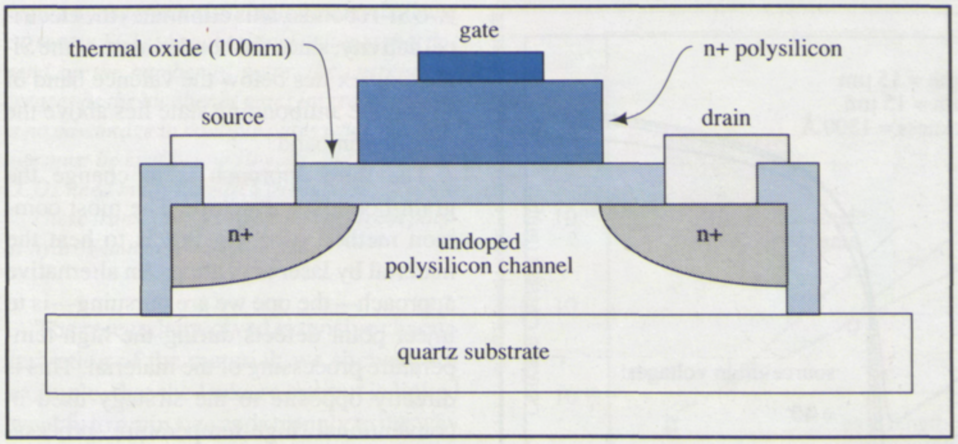


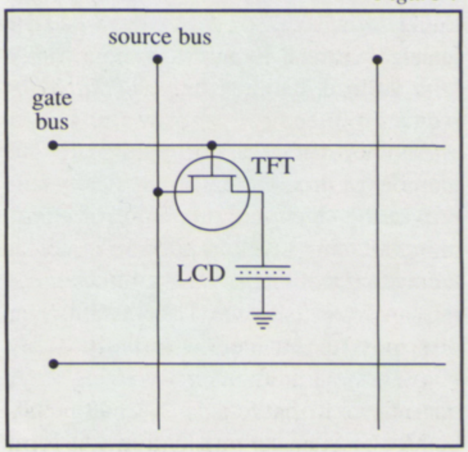
Figure 3. A thin-film transistor (TFT). The channel is generally undoped. If no voltage is applied to the gate, the channel resistance is very high because of the high resistivity of the channel material, and the unbiased TFT is therefore "off". (In that respect the TFT differs from the classical field-effect transistor, in which the "off" resistance is caused by the high resistance of a reverse-biased p-n junction.)

If a positive voltage is applied to the gate, electrons are attracted to the region under the gate; this renders the material conductive and the transistor is turned "on". The "on" processes are very complex because the electrical charge trapped in the grain boundaries of the poly-Si interacts with the electric field introduced by the gate. (This is another way in which this TFT differs from the classical field-effect transistor: the latter is not overly sensitive to structural imperfections.)

Figure 4. A schematic showing a simplified systems application of TFTs. The important characteristic is that the required nonlinear response is handled by the transistor itself.

In front of each pixel electrode there is a transistor which, in a bilevel display (one in which there is no gray scale), acts as a simple switch. The addressing of such an active display follows the process described in the Figure 2 caption. Sufficient voltage to turn on the TFT is applied to the first line, which now is connected to the gate of the TFT. The TFT input (the source) is connected to the column lead; when this is made positive, charge is allowed to flow to the selected pixels. This charge is stored in the pixel element, which has a capacitance of about 1 picofarad per square millimeter. Then all the transistors in the first line are switched off by setting the gate line to zero. The charge is trapped in the pixel; it can leak away only through the finite resistance of the liquid crystal or through leakage of the TFT in the "off" state. If the time required to leak away is equal or greater than the full-frame cycle time of the display, typically 1/60 of a second, the pixel will stay at its full contrast value throughout the addressing cycle. The process is then repeated.

Figure 4



CONTROLLING THE PIXELS WITH THIN-FILM TRANSISTORS

The thin-film transistor is a device that transfers this individual control into the display, and thereby allows the liquid-crystal chemist more freedom in maximizing optically desirable properties.

The layout of a TFT is very similar to that of regular field-effect transistors; the chief difference is in the "off-on" processes (see Figure 3). TFTs have been implemented in a number of materials, but today the only serious contenders for displays are poly-Si and amorphous hydrogenated silicon. (Since poly-Si is commonly used in the construction of integrated circuits, poly-Si-based transistors are also of considerable interest as active devices in three-dimensionally integrated circuits.)

A simplified systems application of these TFTs is shown in Figure 4. The fabrication of a flat color display of modest size—say, 10 x 10 inches—amounts to the fabrication of an integrated circuit 10 x 10 inches in size, with a gate count comparable to the largest random-access modules (RAMs) produced today. This can be done with today's technology, but is still many times more expensive than fabricating a cathode-ray tube.

An advantage of this kind of display is that the pixels can maintain full contrast throughout the addressing cycle, as explained in the Figure 4 caption, thereby dramatically improving contrast and viewing angle of multiline TN LCDs. More importantly, active matrix addressing permits the multiplexing of large guest-host LCDs, which, as I have explained, currently need to be controlled at each individual pixel. Compared to TN LCDs, GH LCDs offer higher contrast, much wider viewing angle, and higher brightness in both reflection and transmission.

Figure 5

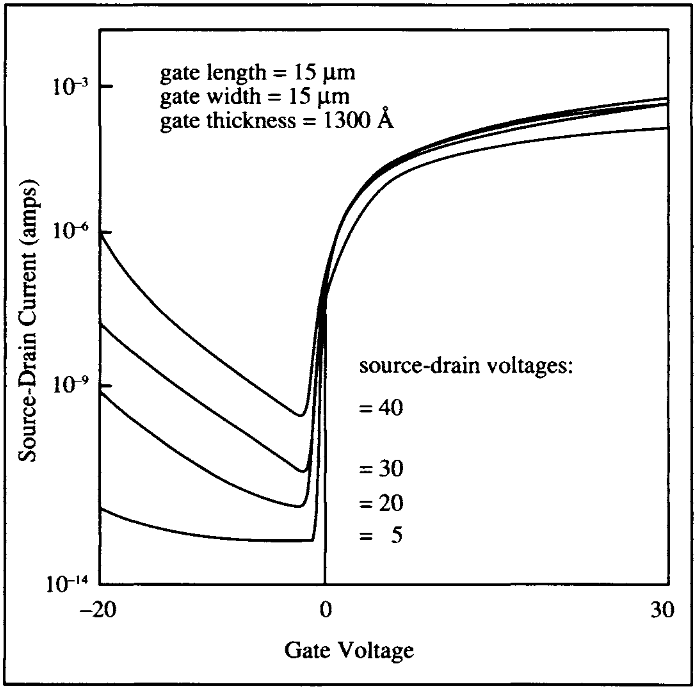


Figure 5. Current flowing through a triple-gated n-type TFT as a function of gate voltage. Data for four different source-drain voltages are shown. The application of 5 volts on the gate changes the current by about seven orders of magnitude. This transistor is one of a series fabricated at the NNF.

GOOD ELECTRONIC PROPERTIES FOR POLY-SI TRANSISTORS

Our research addresses several problems with poly-Si-based transistors.

One is a current-leakage problem that makes it difficult to turn the transistors completely off. The problem arises from grain boundaries that contain regions in which atoms are only marginally bonded. Such "stretched" bonds are roughly a trillion times more likely to be broken by thermal excitation than are the perfect bonds formed in single-crystal silicon. A graduate student, Roberto Proano, and I are conducting research aimed at understanding the origin of this leakage current, and finding ways to reduce it.

There are three ways of reducing leakage current. One method, first used by Seiko, is to make transistors with two gates that are arranged in series so as to reduce the voltage "seen" by each gate. Since the leakage current increases exponentially with voltage, halving the voltage greatly reduces it.

Another method is to hydrogenate the material, a process that dramatically improves the electronic properties of amorphous silicon as well as poly-Si, in which the hydrogenation occurs at grain boundaries. (A student of mine, Timothy Sullivan, discovered the latter effect during the study of polycrystalline silicon solar cells.) A simplified explanation is that marginally bonded Si-Si reacts with hydrogen to form two Si-H bonds. This eliminates the electrical activity, since the bonded state of the Si-H complex lies below the valence band of Si and the antibonding state lies above the conduction band.

The third approach is to change the grain-boundary structure. The most common method of doing this is to heat the material by laser annealing. An alternative approach—the one we are pursuing—is to inject point defects during the high-temperature processing of the material. This is directly opposite to the strategy used in conventional high-temperature processing, which minimizes point defects.

The conventional procedure minimizes point defects because intrinisic point defects cannot easily anneal out of perfect silicon. If they exceed a certain value they tend to precipitate out, resulting in the formation of unwanted defects called stacking faults.

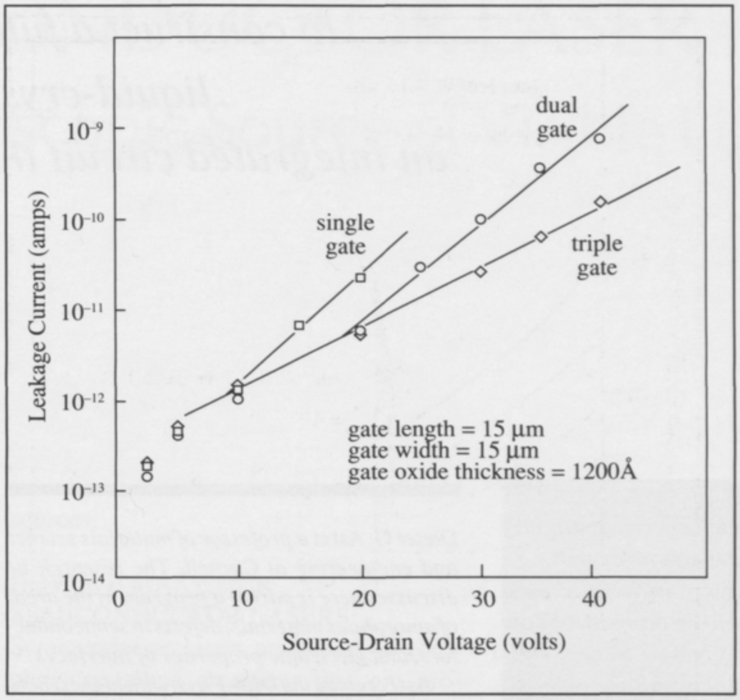
In poly-Si, however, intrinsic point defects migrate to grain boundaries, where they anneal out, enhancing the grain-boundary atomic mobility by permitting climb of grain-boundary dislocations. This has two desirable consequences: the grain size increases and, more importantly, the boundary can achieve a low-energy configuration with a minimum of electrically active broken bonds. We have redesigned the processing cycle to maximize these effects.

The TFTs we have fabricated using this approach meet the electrical requirements of guest-host liquid-crystal displays. Figure 5 shows some results obtained with n-type transistors fabricated by Proano at the National Nanofabrication Facility at Cornell (p-type devices are very similar). These TFTs have exceedingly good transfer characteristics and very low leakage currents at high applied voltages.

Figure 6. The effect of multiple gates on leakage current in TFTs. Above critical voltages that depend on the number of gates, the current decreases as the number of gates increases. There is no advantage in multiple gates when the voltage must be kept below 10 volts, but guest-host LCDs need multiple-gated transistors.

These transistors were fabricated from poly-Si hydrogenated for 30 minutes.

Figure 6



The research involved extensive characterization of the material; we showed, for example, that the leakage current is linked weakly to grain size and strongly to the way grains are aligned relative to each other.

We also investigated the importance of the number of gates and how they are spaced. Results for one, two, and three gates are illustrated in Figure 6. Leakage current was found to decrease as the number of gates increased, provided that the source-drain voltage exceeded a critical value. This critical value was found to be 10, 20, and 30 volts for single, dual, and triple gates; therefore, if the source-drain voltage is kept below 10 volts, as it is in twisted-nematic LCDs, there is no advantage in using more than one gate. On the other hand, guest-host LCDs, which require about 25 volts, need multiple-gated transistors.

An example of an array of TFTs for an experimental display is shown in Figure 7. All the transistors tested were functional and had identical electrical characteristics, and none of the crossovers between source and gate lines were shortened or open.

Figure 7

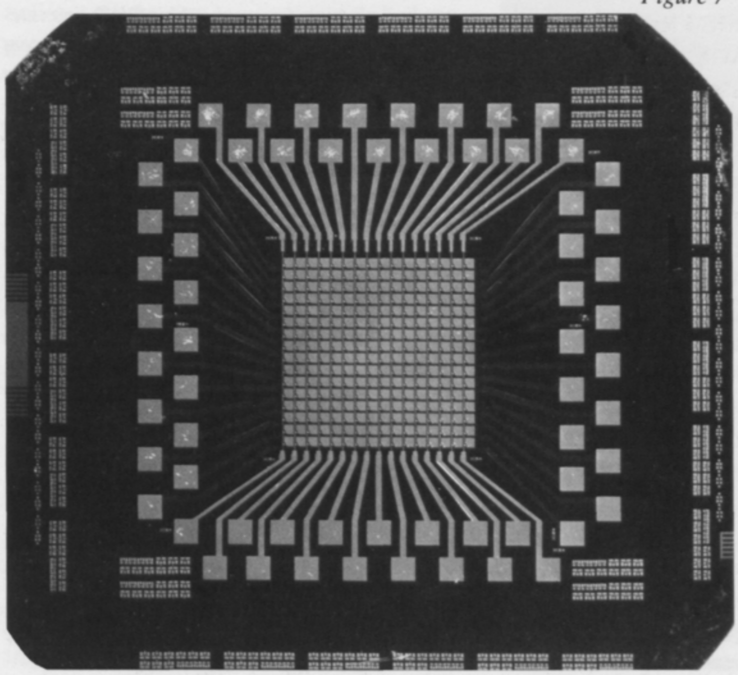


Figure 7. An experimental 16 x 16 display matrix on a three-inch oxidized silicon wafer. The outer squares are contacts. (White markings are scratches from probes.) In addition to the central display, this chip contains numerous test structures on the periphery.

"... to construct a full-sized actively addressed liquid-crystal display is to construct an integrated circuit the size of the display...."

For large flat panel displays, such a TFT array offers a big advantage over currently available liquid-crystal arrays: by putting a highly nonlinear element in front of each pixel, it directly solves the problem of how to meet the nonlinear contrast-versus-voltage requirement. Furthermore, the poly-Si-based transistor has an advantage over other nonlinear elements because it can be made with conventional processing equipment on conventional integrated-circuit lines, and because the same technology can also handle the logic functions required to translate the analog video signal into digitized pixel information—a step that further reduces the number of interconnects.

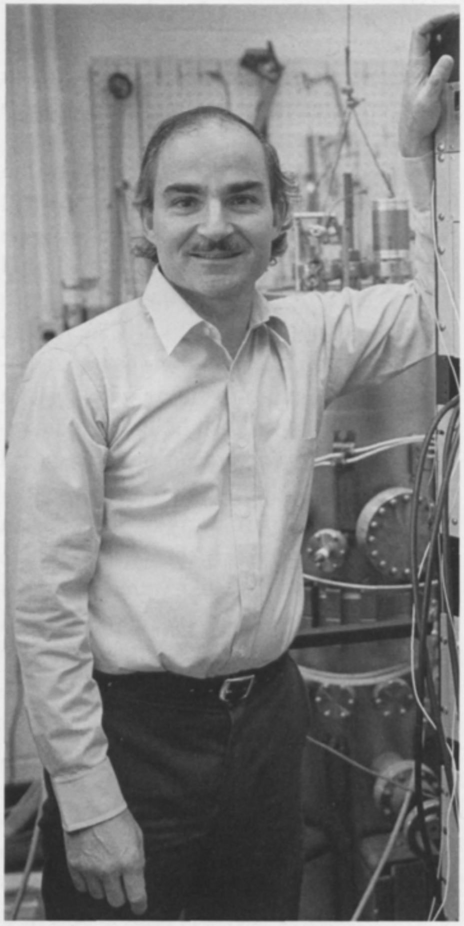
In summary, we can say that to construct a full-sized actively addressed liquid-crystal display is to construct an integrated circuit the size of the display, using non-standard semiconductors and devices. This is still very difficult, but rapid progress is being made worldwide.

Dieter G. Ast is a professor of materials science and engineering at Cornell. The research he discusses here is part of a program in the areas of amorphous materials, defects in semiconductors, and electronic properties of interfaces.

Ast received the Dipl. Phys. with highest honors from the University of Stuttgart, where he studied physics; he received his Ph.D. in materials science from Cornell in 1971. He spent several summers and a sabbatical leave at IBM's T. J. Watson Research Center as a visiting scientist in the semiconductor science and technology department. Subsequently, he spent summers and a second sabbatical at Hewlett-Packard's solid-state laboratory.

During the summers at Hewlett-Packard he worked on active liquid-crystal displays with thin-film transistors fabricated from amorphous silicon. This work is described by Ast in a chapter in Amorphous Hydrogenated Silicon, *recently published by Academic Press as part of the Willardson and Beer series on semiconductors and semimetals.*

The Cornell research described in this article profited from detailed studies of the structure and electrical properties of grain boundaries carried out under DOE sponsorship. The author would like to thank an alumnus, W. Hawkins of the Xerox Corporation, for valuable discussions.



A RED SEMICONDUCTOR LASER

An Efficient Microscopic Source of Visible Light

by J. Richard Shealy

A high-power laser that operates in the visible part of the spectrum and is extremely small has been developed recently in our laboratory at Cornell. It is a semiconductor laser—the most efficient source of light yet discovered—with potential for both research instrumentation and practical applications.

The research usefulness of such a laser is indicated by the fact that the currently available source of comparable emission (used by several groups on campus) is the Kr^+ ion laser, which is housed in an instrument about ten feet long and requires a large power supply. Our red laser is roughly a thousand times more efficient and ten thousand times smaller.

One application would be in holographic scanners, such as those at supermarket checkout counters; the semiconductor red lasers would replace the gas lasers now used. Automobile manufacturers are interested in semiconductor red lasers for tail lights and, especially, to meet the future requirements for brake lights mounted on windshields, where small size would be an advantage.

Some of the funding for our research comes from Kodak, which has, of course, an interest in advanced-technology light sources.

HOW WE MAKE OUR SEMICONDUCTOR LASERS

Semiconductor lasers are based on complex crystalline structures that are produced in a crystal-growth reactor. Cornell's activity in semiconductor crystal growth goes back some fifteen years (in work directed by Professor Lester Eastman), but the modern techniques used for visible lasers have been developed, in my Phillips Hall laboratory, only in the past year. We plan to open a larger facility soon.

We have designed and built a specialized vapor-phase growth reactor in which we can control the properties of a very thin semiconductor layer. In fact, the best red lasers currently have an active region that is only 20 to 50 atomic layers in thickness. Our measurements of this ultrathin layer are augmented by images (see Figure 1) prepared by transmission electron microscopy by Professor Barry Carter and his associates at Cornell's Materials Science Center.

The structure operates by injecting electrons and holes into the very thin active

Figure 1

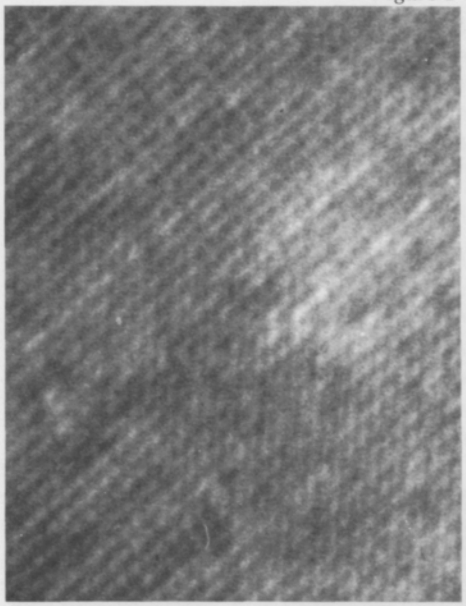


Figure 1. A micrograph of a semiconductor superlattice illustrating the dimensional control of the crystal-growth process. The ultrathin semiconductor layers are two atomic layers in thickness. The "rows" in the image are about 2.8 angstroms apart; each represents one atomic layer.

The transmission electron micrograph was prepared at Cornell's Materials Science Center by Professor Barry Carter.

"Our red laser is roughly a thousand times more efficient and ten thousand times smaller [than the currently available source]."

Figure 2

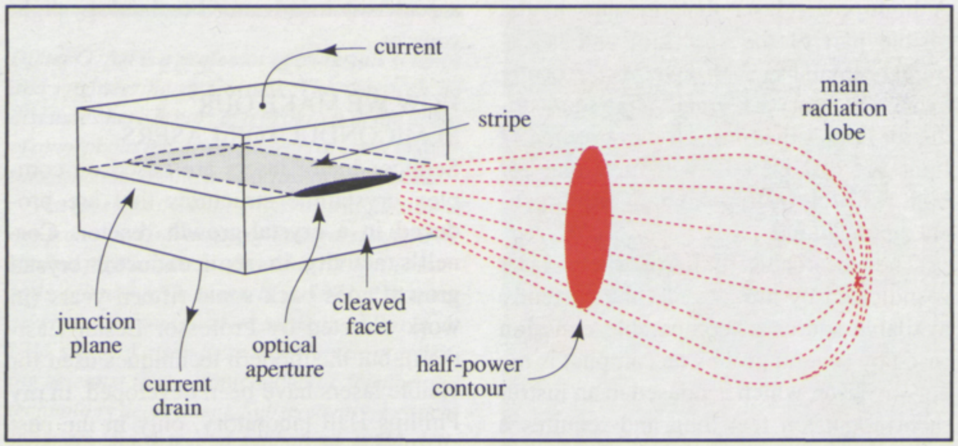
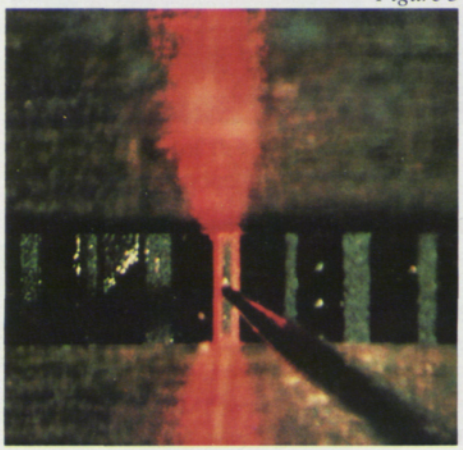


Figure 2. The radiation pattern of the semiconductor red laser. The light emanates from the thin active region in the "sandwich" structure, and is emitted from the cleaved facet. The radiation pattern is elliptical in the vertical plane.

Figure 3. An optical micrograph of a series of visible layers (metallic stripes) on a cleaved bar. The laser is emitting red beams of light from either end. The length of the bar visible in the micrograph is about 220 μm. Also visible is a microprobe through which the diode current passes.

Figure 3



region. This is done by placing the crystal structure between layers of n-type material (the source of electrons) and p-type material (the source of holes), and passing a current through the diode. The electrons and holes annihilate each other with emission of a photon.

Lasing action ensues as a result of an optical cavity that has been formed in the structure with the use of standard microfabrication techniques (available at the National Nanofabrication Facility and other on-campus facilities). Such a cavity, in the form of a stripe, is indicated in Figure 2, and such stripes are visible in the Figure 3 micrograph. When the semiconductor crystal is appropriately cleaved, crystalline faces normal to the surface of the grown semiconductor layer are exposed normal to each stripe, and these form a resonant cavity with mirror-like surfaces. After several passes, the light is amplified to the point at which lasing occurs.

A BRIGHT FUTURE FOR A NEW KIND OF LASER

Semiconductor lasers offer some important advantages over alternative light

sources. They are efficient: in some cases the efficiency of conversion from electricity to light exceeds 55 percent (by comparison, the efficiency of a conventional incandescent bulb is less than 1 percent). And they are small, typically a few hundred square micrometers in size.

Our red laser has additional advantages for certain applications: it operates in the visible region with impressive power output. A device similar to the one illustrated in Figure 3 has yielded powers exceeding 1.4 watts, which is comparable to the emission from the large-frame ion lasers now in use.

The larger significance of this development is the prospect of using the new techniques to fabricate a variety of lasers with "customized" properties. Semiconductor lasers promise to be adaptable and highly useful for applications at hand and for others still to be developed.

J. Richard Shealy became an assistant professor of electrical engineering at Cornell this year after earning his doctorate here in 1983 and continuing as a research associate.

He received the B.S. degree in electrical engineering from North Carolina State University in 1978 and the M.S. in electrophysics from the Rochester Polytechnic Institute in 1980. While he was an undergraduate, he served as a research assistant in solid-state physics at the Research Triangle Institute, and while he was a graduate student he was a member of the technical staff at General Electric.

"Our red laser has additional advantages . . . it operates in the visible region with impressive power output."

SPEEDING UP THE ELECTRONS IN SEMICONDUCTOR TRANSISTORS

by Paul J. Tasker and Lester F. Eastman

A major thrust in the drive to improve the performance of electronic devices is to increase the transit time of electrons. There are two approaches: decrease the size of the structure, so the electrons have shorter distances to traverse; or use materials, such as the semiconductor gallium arsenide, that have better electron-transport properties.

Part of the effort of our group at Cornell is to optimize the performance of transistors whose materials include GaAs and related compound semiconductors. One type, for example, is the *metal-semiconductor field-effect transistor* (MESFET), in which the charge flow is controlled by an electric field applied to a metal gate between the current source and the drain. The *channel*—the active area under the gate—is composed of semiconductor material that has been *donor-doped* (that is, impurities have been introduced to change the electrical conductivity). Advanced types have interfaced layers of different compound semiconductors to further improve the electron-transport properties.

Figure 1

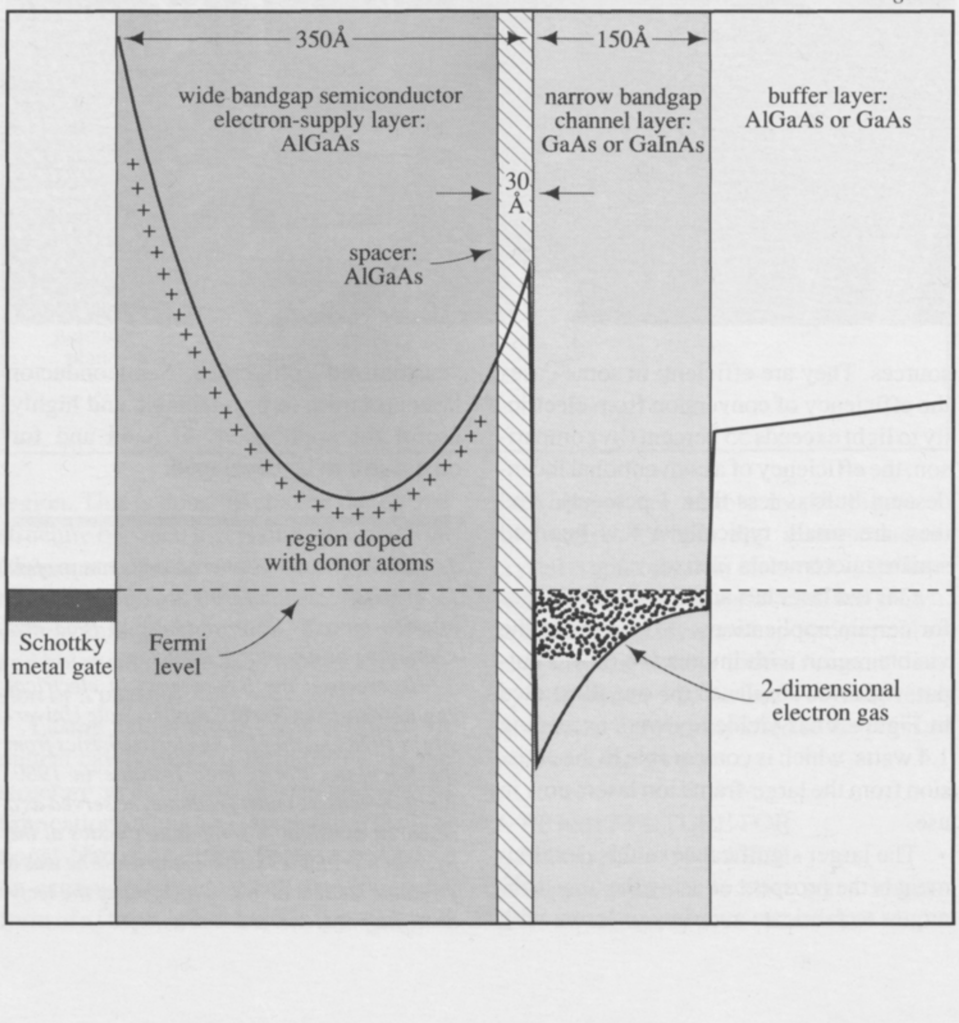


Figure 1. Potential profile of the conduction band of a modulation-doped heterojunction.

"Recently this work has produced a transistor with a picosecond (10^{-12} second) transit time, the fastest ever reported."

MODULATION DOPING OF SEMICONDUCTOR FETS

The performance of doped-channel GaAs MESFETs has improved significantly as the gate length has been reduced to submicron dimensions (one micron = 10^{-6} meter). However, as the gate dimension is reduced, the dimensions of the doped GaAs layer—whose donor atoms provide electrons—must also be scaled. A difficulty arises: reduction of the thickness of the active channel creates a need for higher doping densities, and the resulting increased scattering of electrons reduces their average velocity. This offsets the improvements that can be achieved by scaling down the gate dimension.

To produce short transit times in transistors with submicron gate lengths, it is important, therefore, that the donor atoms be removed from the path of the electrons. This can be achieved by using an abrupt interface, called a *heterojunction*, between two compound semiconductors with different bandgaps. The dopant atoms are placed in the semiconductor that has the larger bandgap, and the electrons transfer to the semiconductor with the narrower bandgap, as shown in Figure 1. An undoped spacer layer is often included in the wide-bandgap semiconductor to further increase the separation between the electrons and the donor atoms. The transferred electrons are confined near the heterojunction by the potential well. Their energy levels are quantized in one dimension, and so a two-dimensional electron gas results.

This process is referred to as *modulation doping*; hence, transistors with such a structure are called *modulation-doped field-effect transistors* (MODFETs)*. The epitaxial growth of high-quality modulation-doped structures has been achieved by molecular-beam epitaxy (MBE).

Researchers in our group, in cooperation with Richard C. Tiberio and Edward D. Wolf of the National Nanofabrication Facility at Cornell, were the first to demonstrate superior performance of submicron-gate-length transistors fabricated from structures of this kind. Recently this work has produced a transistor with a picosecond (10^{-12} second) transit time, the fastest ever reported.

*MODFETs are also referred to as HEMTs (high electron mobility transistors); SDHTs (selectively doped heterojunction transistors); and TEGFETs (two-dimensional electron gas field-effect transistors).

ASSESSING THE PERFORMANCE OF SEMICONDUCTOR FETS

An important indicator of merit relating to speed and frequency performance is a quantity called the *intrinsic unity current gain cut-off frequency*, f_T. This is assumed to be given by

$$f_T = \upsilon_{SAT} \div 2\pi L_g \qquad (1)$$

where υ_{SAT} is the saturated velocity of electrons in the semiconductor and L_g is the gate length of the transistor.

We made a study of our own and other published data in order to determine the maximum saturated electron velocity for several MODFET material systems. The results (Figure 2) indicate that the pseudomorphic AlGaAs/GaInAs MODFETs are superior to the conventional AlGaAs/GaAs MODFET at all gate lengths.

As the gate length is reduced, however, the fitted curves passing through the data points diverge from the linear curve with a gradient of −1 that is predicted by Equation 1. Figure 3 shows that the simple relationship predicted by Equation 1 is valid pro-

Figure 2. Summary of state-of-the-art results for submicron-gate-length MODFETs. Each of the three types represented has a layer of AlGaAs and a compound semiconductor layer with a different composition.

The data points were obtained from papers published by researchers from several universities and companies: Cornell (labeled CU), General Electric (GE), Hewlett -Packard (HP), Nippon Electric Corporation (NEC), Siemens (SE), Toshiba (TOS), and the University of Illinois (UI).

Note that the fitted curves are not linear, as predicted by the generally assumed relationship of Equation 1. Linearity is exhibited (see Figure 3) when the gate length is "corrected" for various factors that influence the measured f_T.

Figure 3. Replotted Figure 2 data, using "corrected" gate lengths. These fitted curves show the linearity predicted by Equation 1.

vided that L_g is replaced by $L_g + \Delta L$. The additional amount, ΔL, compensates for effects (fringing capacitance, pad capacitance, and output RC time constants) that reduce the measured f_T.

The measured saturated velocities (υ_{SAT}) are simply obtained from the gradient of plots such as those in Figure 3. The values calculated for three different layered MODFETs are indicated. They are all larger that the values obtained for the doped-channel GaAs MESFET, but they are smaller than the value that was originally predicted. There were other unexplained effects: Analysis of microwave data showed that f_T, and hence υ_{SAT}, was also a strong function of gate bias potential (going through a maximum). And the peak value of f_T, and hence υ_{SAT}, increased as the thickness of the spacer layer decreased (Figure 4a) and as the concentration of indium increased (Figure 4b).

Figure 2

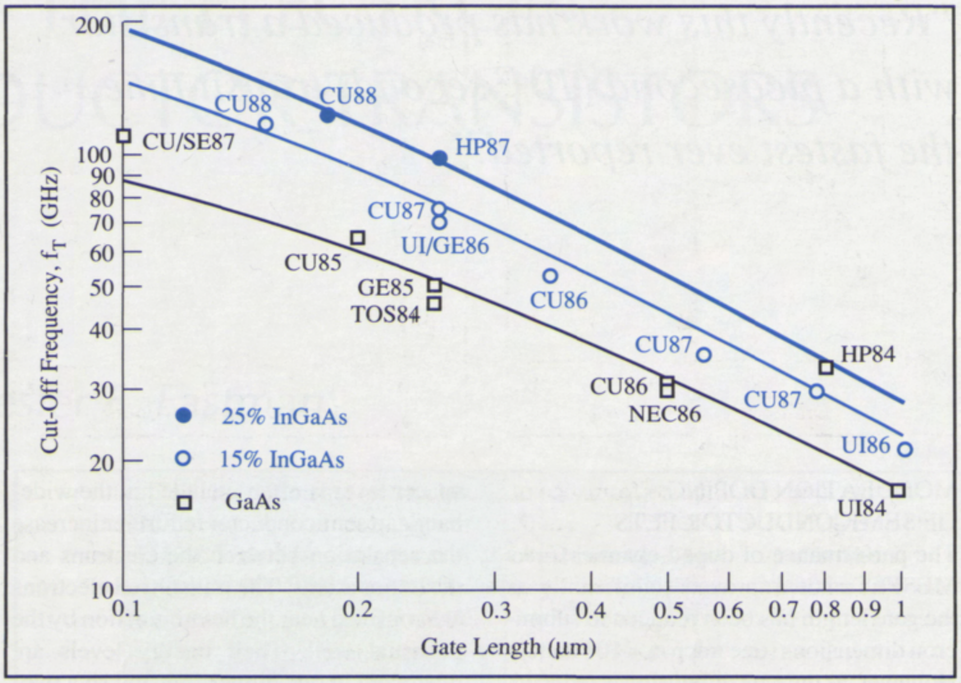


Figure 3

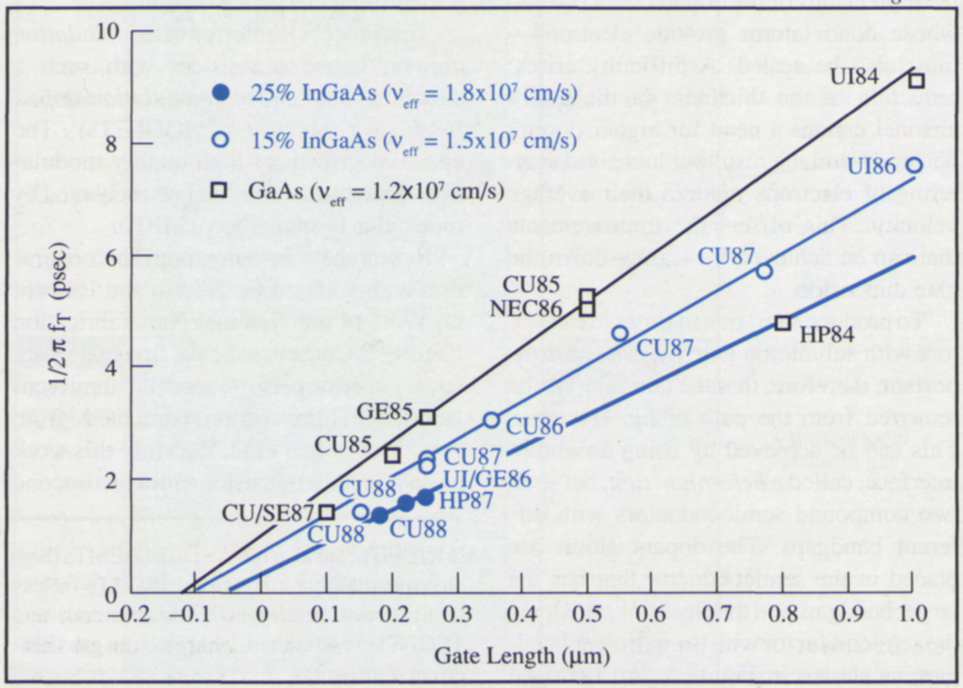


Figure 4a

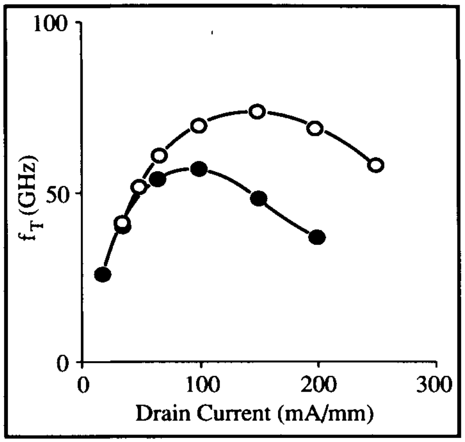


Figure 4b

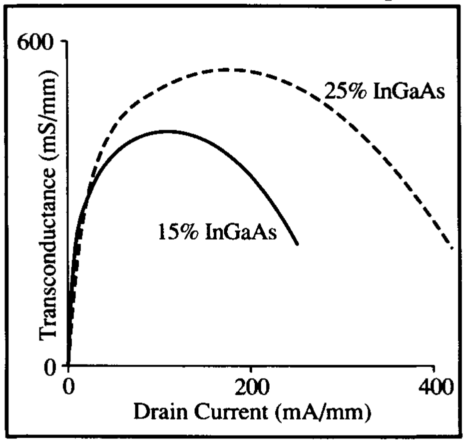


Figure 4. Several factors affecting the measured f_T.

In 4a, measured f_T is plotted versus drain current for two $Al_{0.3}Ga_{0.7}As/GaAs$ MODFETs. Both have gate lengths of 0.2 µm, but they have spacer layers of different thicknesses.

In 4b, transconductance, which is proportional to f_T, is plotted versus drain current for two $Al_{0.3}Ga_{0.7}As/Ga_{1-y}\,I_y\,As$ MODFETs. Both have gate lengths of 0.2 µm, but they have different indium content. The drain voltage is fixed (at 1.5 volts); gate potential varies to change the current.

We conclude that if the performance of nanometer-gate-length MODFETs is to be optimized, the cause for the low measured velocities and their sensitivity to layer parameters (thickness of the spacer layer, indium composition, and gate bias potential) must be understood.

THE ADDITIONAL FACTOR OF MODULATION EFFICIENCY

In the field-effect transistor, the drain current, I_D, is modulated by varying the number of electrons, Q_{TOT}, in the active layer below the gate. It is generally assumed that in submicron-gate-length transistors, all charge modulated by the gate travels at the saturated velocity; hence, f_T is given by Equation 1.

However, all the charge modulated by the gate does *not* travel at the saturated velocity. A more complete expression for f_T, one that accounts for this effect, has been developed by researchers in our group:

$$f_T = \frac{\upsilon_{SAT}}{2\pi(L_g + \Delta L)} ME = \frac{\upsilon_{eff}}{2\pi(L_g + \Delta L)} \quad (2)$$

Here the term ME, for modulation efficiency, has been added to Equation 1, and a new velocity measure, υ_{eff}, is defined. The actual gate length, L_g, is corrected to $L_g + \Delta L$, in accordance with the considerations discussed in connection with Figure 3. The added term ME quantifies how efficient the transistor is in utilizing the charge modulated by the gate; it is defined as

$$ME = \partial Q_{SVM} \div \partial Q_{TOT} \quad (3)$$

where Q_{SVM} represents the amount of charge that the gate would have to modulate to get the same drain current if all the charge did travel at the saturated velocity.

The measured velocity determined from f_T data is, in fact, υ_{eff} and not υ_{SAT}. The value of υ_{eff} can vary with both layer structure and gate bias potential, since ME is a function of these parameters.

In our laboratory, ME has been modeled for both the conventional $Al_{0.3}Ga_{0.7}As$/GaAs MODFET and the pseudomorphic $Al_{0.3}Ga_{0.7}As/Ga_{0.85}In_{0.15}As$ MODFET. The results (Figure 5) demonstrate that it is the variation of ME with gate potential that explains the experimental observations.

Analysis of these results shows that it is the interaction of two different mechanisms for inefficient charge control that accounts for the variations in high-frequency performance observed in the MODFETs. One mode is dominant at low drain currents (near pinch-off) and the other is dominant at high drain currents (open channel).

The interpretation is as follows. Since the electron velocity is nonuniform under the gate, current continuity requires that additional charge be present in the channel containing the two-dimensional electron gas (see Figure 1). It is the modulation of this additional charge component that becomes dominant at low levels of drain current. When the sheet density of the electron gas is high, the electrons are also thermally excited into the potential dip that is present in the high-bandgap electron supply layer (see Figure 1). As a consequence, the gate potential has to modulate both high-velocity charge in the two-dimensional electron gas, and the low-velocity charge in the electron supply layer. It is the modulation of this additional charge component that becomes dominant at high drain currents.

Neither of these mechanisms, on its own, would limit to less than 1.0 the maximum ME achievable in any transistor structure, but when they interact, *ME can* be limited to values below 1.0. As a consequence, the maximum *ME* that can be achieved—and hence the maximum measured f_T—is a sensitive function of the layer structure. Figure 5 shows examples. The inference is that the velocity extracted from the measured f_T of MODFETs now being fabricated is definitely not υ_{SAT}. Instead, it is an effective velocity, υ_{eff}. The simulations indicate that a saturated electron velocity as high as 2.0 x 10^7 centimeters per second is actually necessary to explain the measurements. The low value of maximum *ME* occurring in MODFET structures accounts for the low observed velocities.

FURTHER ADVANCES IN TRANSISTOR DESIGN

This information provides a clue as to what must be done to keep transit times short when gate lengths are short. MODFET layers must be designed so as to maximize the density of the two-dimensional electron gas and minimize parasitic charge modulation. It should be possible to fabricate structures in which performance actually is limited by the transit time of electrons— a half picosecond at nanometer gate lengths (>100 nm).

Cornell is an excellent place to carry out

Figure 5a　　Figure 5b

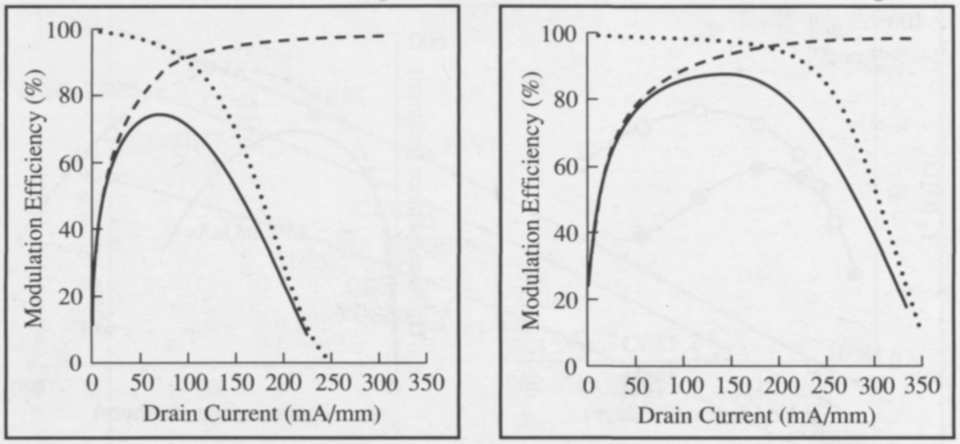
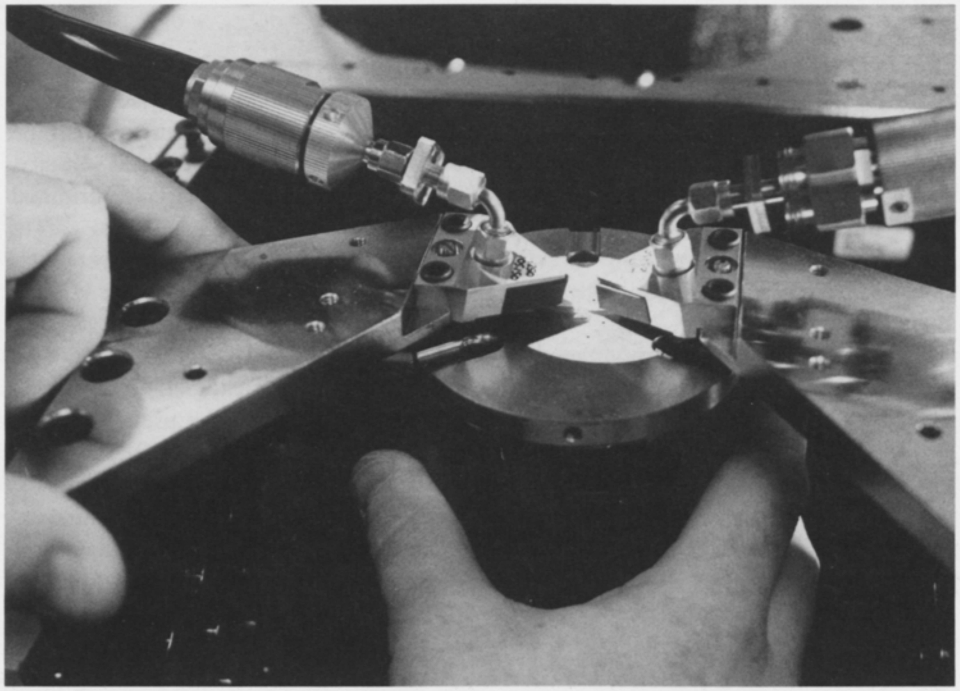
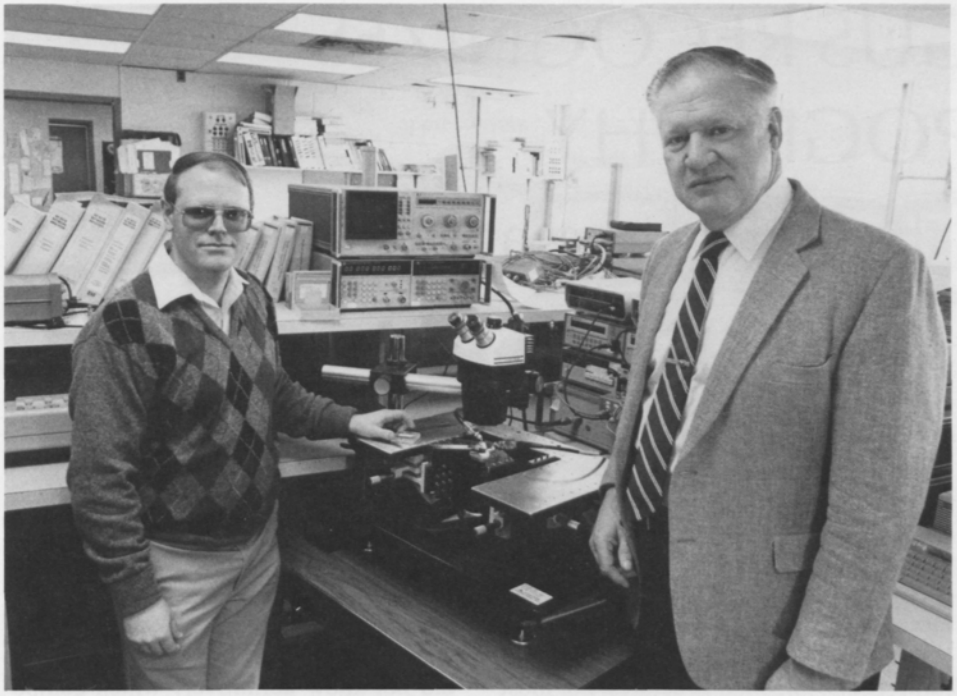


Figure 5. Curves for computed modulation efficiency as a function of drain current for (a) conventional $Al_{0.3}Ga_{0.7}As/GaAs$ and (b) pseudomorphic $Al_{0.3}Ga_{0.7}As/Ga_{0.85}In_{0.15}As$ MODFETs. The dashed envelope includes only the effect of nonuniform velocities under the gate. The dotted envelope includes only the effect of parasitic supply charge. The solid curve includes both, and their interaction.

Below: In the laboratory at Cornell, a device is under test at microwave frequencies.





Above: Tasker (on the left) and Eastman use this microwave measuring equipment in their research.

a program of this kind. The facilities available here provide a unique combination of equipment and technology for the growth of compound semiconductor materials, for submicron lithography, and for characterization and analysis of microwave transistors. They have substantially advanced the state of the art of MODFET transistors.

Paul J. Tasker is a senior research associate who works in Professor Lester F. Eastman's laboratory at Cornell's School of Electrical Engineering.

A native of the Isle of Man, Tasker holds two degrees from Leeds University: the B.Sc. in physics and electronics with first-class honors, awarded in 1976, and the Ph.D. in electrical and electronics engineering, awarded in 1983. He has been at Cornell since then, conducting research in the areas discussed in this article, serving as a consultant to a number of industrial researchers, and occasionally helping to teach in the undergraduate and graduate programs.

Eastman, who is the Given Foundation Professor in Engineering, was educated at Cornell (B.E.E. 1953, M.S. 1955, Ph.D. 1957) and joined the faculty after completing his doctorate. Beginning in 1964, he developed a research concentration in solid-state devices; currently his research is conducted partly in association with the National Nanofabrication Facility.

Eastman has chaired many national and international workshops, conferences, and symposia, and originated the biennial IEEE–Cornell Conference on Microwave Semiconductors, which has been held on campus since 1967. He has spent leaves at Chalmers Technical University in Sweden, the RCA Research Laboratory, Lincoln Laboratory at the Massachusetts Institute of Technology, the IBM Research Laboratory, and Cayuga Associates, a development firm he helped establish in Ithaca. He is also active as an industrial consultant. He is a fellow of the Institute of Electrical and Electronics Engineers and a member of the National Academy of Engineering.

The authors would like to acknowledge the important contributions of Stretch Camnitz, Loi Nguyen, Mark Foisy, Dave Radulescu, and William Schaff. This work was supported in part by the United Technologies Research Center, the Harris Corporation, Martin Marietta Laboratories, the Office of Naval Research, the Army Research Office, and the Joint Services Electronics Program.

HOW A FUNGUS RECOGNIZES SURFACE TOPOGRAPHY

A Problem Solved through Microfabrication

by Harvey C. Hoch and Richard C. Staples

Microfabrication can contribute to cellular science as well as to electronics or the study of inorganic material surfaces. Take, for example, our study of a bean-rust fungus, which was carried out partly at the National Nanofabrication Facility (NNF) at Cornell. Microfabrication enabled us to find out how the fungus navigates across a leaf surface to find the right place to penetrate its host; and, more importantly, it provided us with a wealth of information about how the fungus might be controlled.

The critical piece of information, it turned out, is that a certain topographical feature of the leaf surface is necessary for successful invasion by the fungus. The feature is a ridge very close to 0.5 micrometer (μm) or millionths of a meter in height. We were able to discover this, and learn about related biological processes, by taking advantage of the resources and expertise available at the NNF.

THE BIOLOGICAL BACKGROUND: HOW FUNGI CAUSE DISEASE

Many plant diseases are caused by fungi. When such microorganisms penetrate the plant surface, they grow within the tissues for a period of time, utilizing the nutrients found there, and then they reproduce within the plant or on its surface to form new *propagules*, or spores. When transported to other plants, these spores can repeat the disease cycle.

To invade the host plant, fungi must first form special infection structures. For most fungi, this initial infection structure is an *appressorium*, a swollen cell of the fungus that helps it to adhere to the plant surface while it develops another specialized structure, the *penetration peg*. This structure is involved in the actual penetration of the *epidermis*, the outer cell layer of the plant.

The fungus we studied belongs to an economically important group known as *rust fungi* (because of the rust-colored areas on the leaf surface created by the mass of spores). Rust fungi can invade the host plant only through *stomata*—pores in the epidermis of the leaf through which gas exchange with the surrounding atmosphere occurs. The fungi germinate from spores on the leaf of the host (for example, a bean plant) and grow toward stomata, where they cease growth and develop appressoria (Figure 1). How the fungal pathogen recognizes when it is at the stomatal opening has been the subject of our investigation.

OBSERVING FUNGAL GROWTH ON FABRICATED SURFACES

We knew from previous research that the fungus somehow senses a certain topography that triggers the development of the appressorium. Until recently, however, we did not know definitively which component of the stomata contained the topographical signal, what the signal dimensions were that induced appressorium formation, or how the fungal cell sensed the signal. With the tools we had available to us, we were not able to address these important questions, so we sought assistance from the NNF.

The idea was to microfabricate topographical signals that had precise dimensions and spacings (ridges, grooves, etc.) so that we could find out what topographical features are signals for appressorium formation. To accomplish this, templates were fabricated from silicon wafers by electron-beam lithography and reactive-ion etching, and then polystyrene replicas were made by heat-pressing polymerized styrene onto the templates.

When the rust fungus was grown on the polystyrene replicas, it responded to the various topographies in ways that indicated

Figure 1.

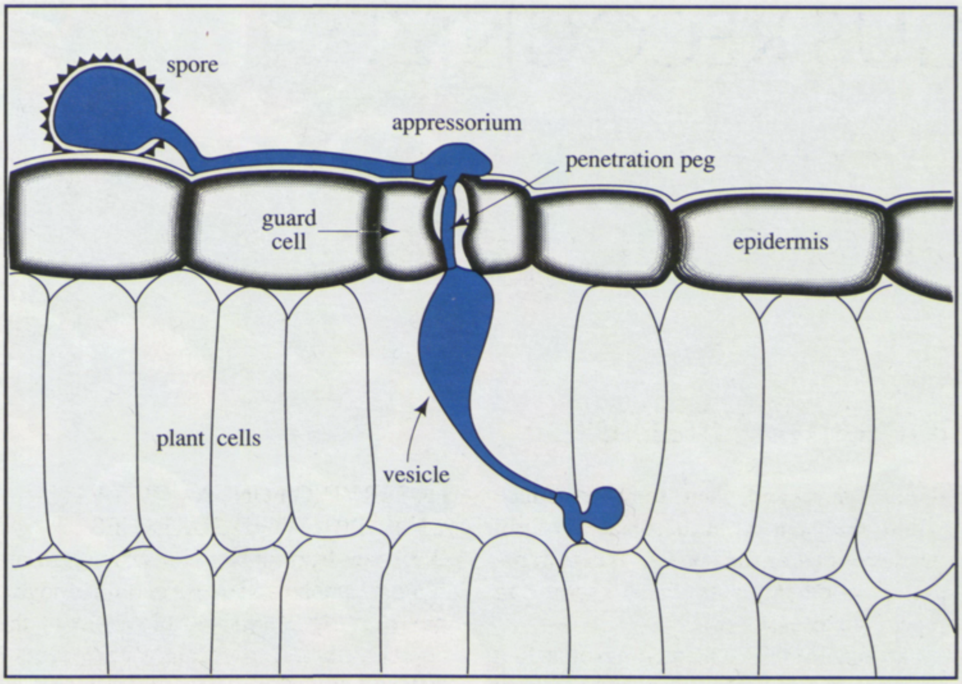


Figure 1. A diagrammatic representation of infection structures produced by the bean-rust fungus on the surface of a leaf. The fungus germinates from the spore, grows toward a stoma—a pore in the leaf's epidermis—and develops into an appressorium. A penetration peg enters the stoma past its guard cells. Nutrients are removed through a vesicle and connected structures.

Figures 2 and 3 on the following page show the similarity between appressoria on a leaf and appressoria formed on polystyene replicas with ridges of the correct size.

Table I. Appressorium formation by the bean-rust fungus in reponse to topographical ridges of varying dimensions.

Ridges height x width, µm	*Percent Appressoria*
0.03 x 2.0	0.00
0.1 x 2.0	5.75
0.25 x 2.0	4.75
0.5 x 2.0	75.35
1.0 x 2.0	8.75
2.0 x 2.0	0.00
0.5 x 0.5	71.21
0.5 x 1.0	69.00
0.5 x 2.0	72.60
0.5 x 4.0	76.40
0.5 x 100*	69.40
5.0 x 100*	0.20

*Polystyrene replicas of 0.5 or 5.0 µm x 100 µm x 100 µm

to us which surface features were most important for triggering the formation of the infection structure on plant leaves. The results are summarized in Table I.

We found that the maximum number of appressoria were formed in response to ridges or plateaus 0.5 µm high. Appressoria that formed on these ridges were morphologically and functionally similar to those formed over stomata (Figures 2 and 3). The percentage of appressoria observed for rust germlings responding to ridges more than 1.0 µm or less than 0.25 µm in height was significantly lower than that for the 0.5-µm-high ridges. Since the diameter of rust germling cells ranges between 5.0 and 8.0 µm, the optimum signal height for appressorium formation is, therefore, between one-tenth and one-sixteenth of the cell size.

As the data in Table I show, the width of the ridge did not constitute an important parameter of the signal. This was especially apparent when plateaus 100 µm square, arranged in a checkerboard pattern, were examined. Germlings growing either onto or off these plateaus developed appressoria only at the edges of the plateaus, and only when they were 0.5 µm high. Furthermore, essentially no cell differentiation (0.20 percent) occurred on replicas of 5.0-µm-high plateaus.

All these data, considered together, indicated to us that the signal for appressorium formation was an elevation change of approximately 0.5 µm, and that two acute angles must be present. The presence of only one angle—such as that associated with the top or the bottom of the 5.0-µm plateaus or ridges—did not serve as an inductive signal. Instead, the rust cell simply grew over the obstacle, usually with poor contact on the leading edge (see Figures 4 and 5).

COMPARING SYNTHETIC AND NATURAL SURFACES

The discovery that the signal for appressorium formation consists of a sharp change in the elevation of the substrate surface by

Figure 2

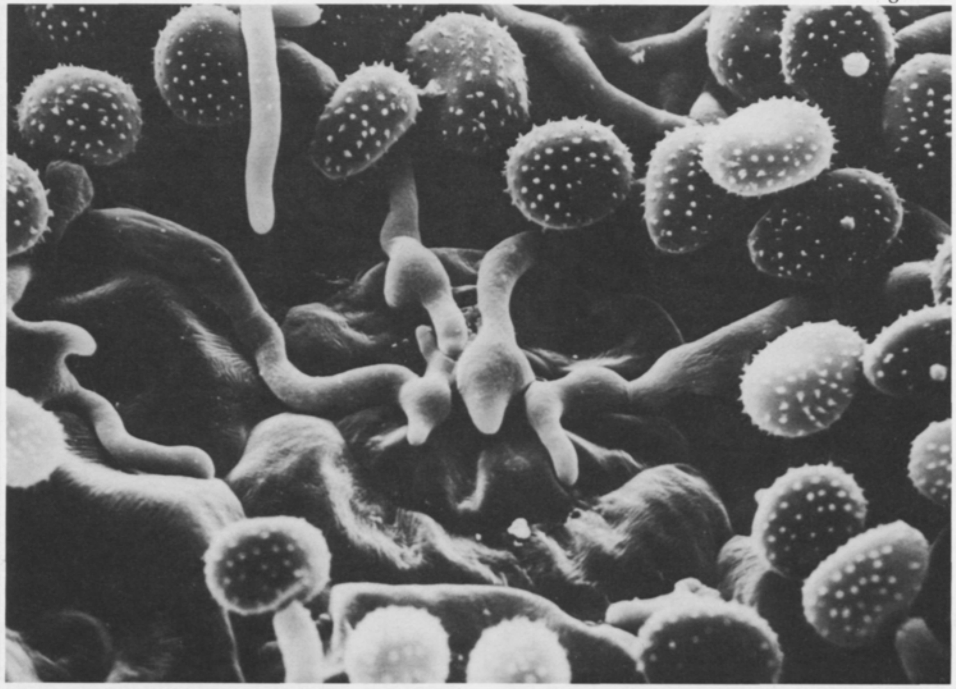
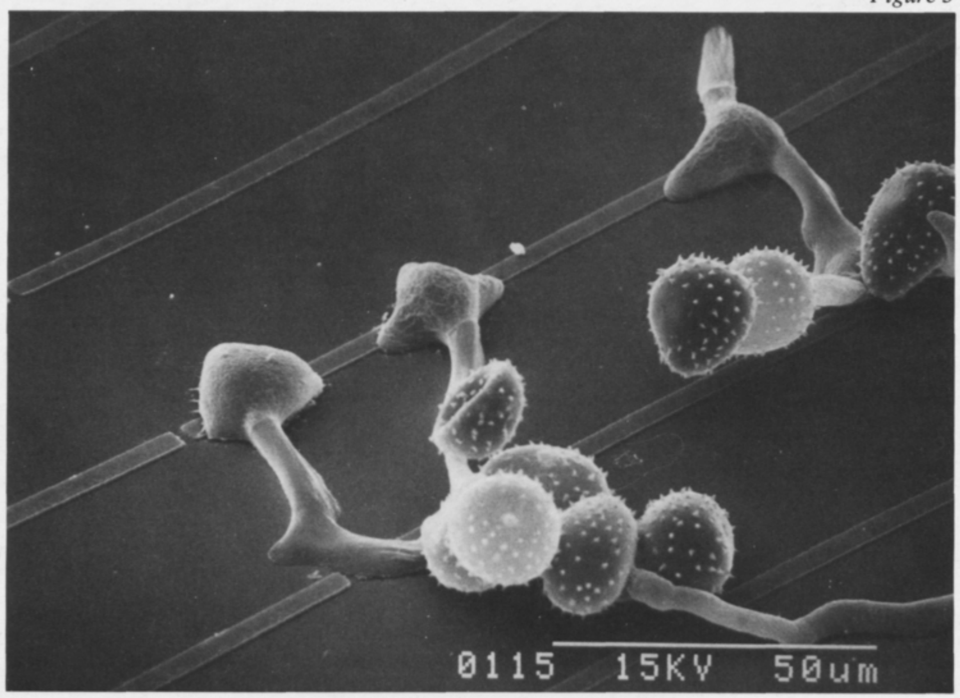


Figure 3



"How the fungal pathogen recognizes when it is at the stomatal opening has been the subject of our investigation."

Figure 2. Directed growth of several bean-rust germlings on a leaf. All these germlings grew toward the same stoma, which is obscured by the developing appressoria.

Figure 3. A polystyrene replica containing ridges 0.5 μm high and 4.0 μm wide. These ridges induced appressorium formation in the bean-rust fungus.

Figures 4 and 5. Growth of fungus germlings on polystyrene replicas with ridges 5.0 μm high and 4.0 μm wide. Appressorium development was not induced. Instead, the fungus germlings grew over them.

Figure 6. A scanning electron micrograph of bean-leaf stomatal guard cells. The prominent erect lips serve as the signal for appressorium formation in the fungus.

Figure 4

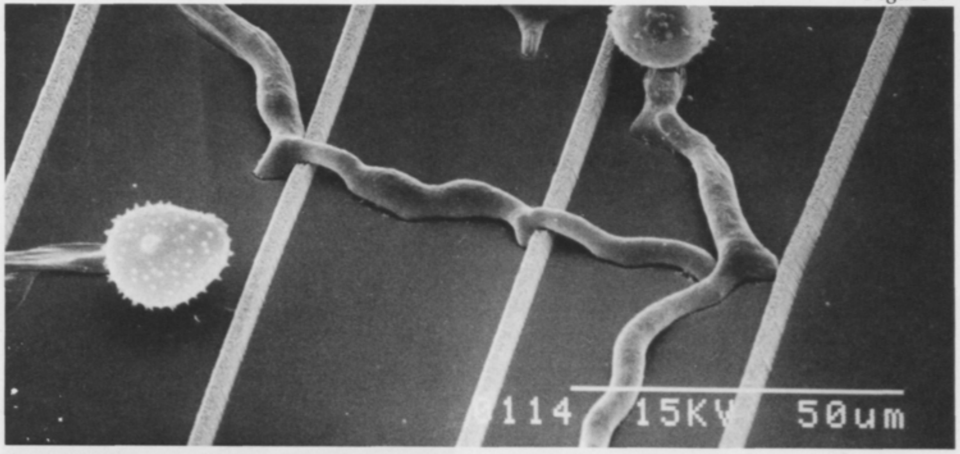


Figure 5

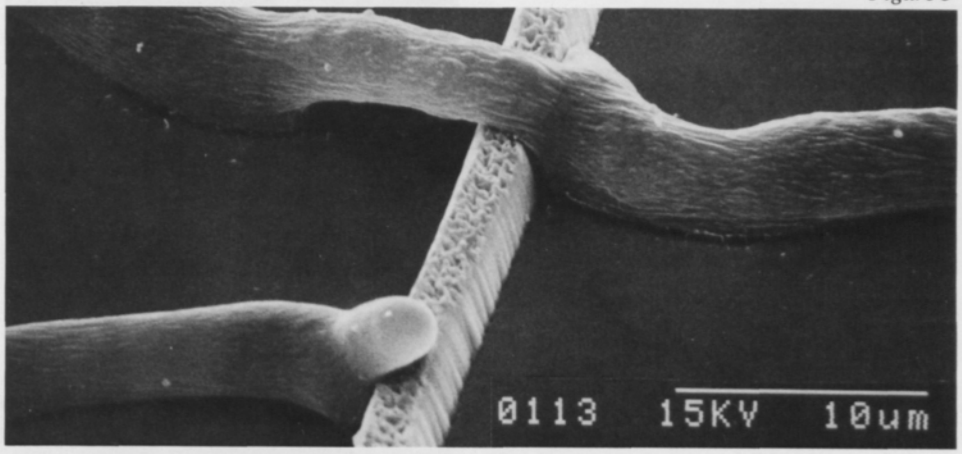
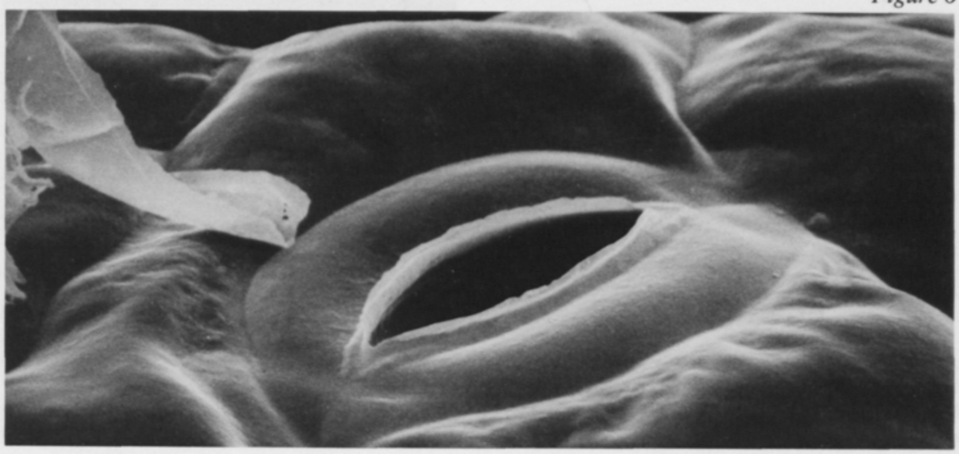


Figure 6



0.5 μm led us to reexamine the morphology of the bean leaf to determine whether similar topographies exist. Scanning electron microscopy of cryogenically prepared bean-leaf specimens revealed prominent protrusions surrounding the stomata (Figure 6). These protrusions were formed by specialized cells, called *guard cells*, which had "lips" oriented nearly perpendicular to the cell surface. The mean height of the lips turned out to be 0.487 μm—very close to the optimum height we had deduced from our experiments with the fabricated polystyrene ridges.

The rust fungus must not only recognize appropriate sites (stomata) for infection structures, but also find these sites without expending unnecessary energy growing aimlessly over the leaf surface. Thus, growth is oriented toward the stomata. Using polystyrene replicas of silicon wafers containing uniform but variously spaced topographical ridges, we found that rust germlings responded with oriented growth. When the ridges were 0.5 μm high by 1.4 μm wide and spaced 0.5 μm to 15.5 μm apart, the germlings grew in a very straight line right across the ridges. As the spacing increased, however, the straightness diminished; spacings of more than 30 μm generally did not serve as efficient signals for the fungus to continue growing perpendicular to the ridges. Examination of the leaf shows that many of the surface valleys, formed by the merging of the epidermal leaf cells, are arranged in semiconcentric patterns around the stomata. These valleys are appropriately spaced to serve as efficient signals for guiding the rust germlings to the stomata.

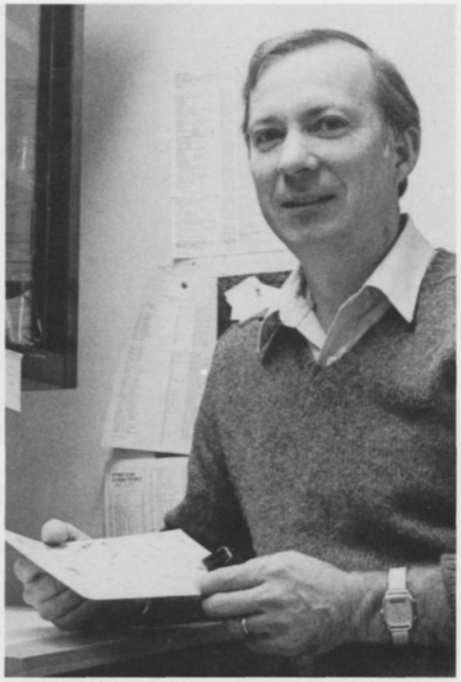
MICROFABRICATION AS A TECHNIQUE FOR BIOLOGISTS

The results of this study, which would not have been possible without the microfabrication capabilities of the NNF, have revealed an approach to the control of the bean-rust fungus. Already scientists are seeking ways to engineer plants with stomatal guard-cell lips with dimensions that do not trigger appressorium formation when the fungus grows over stomata.

Controlling plant disease through an alteration of plant morphology represents an important addition to the arsenal of conventional disease-control mechanisms that rely heavily on pesticides. And beyond this kind of application is a broader range of possibility. Integration of the cellular sciences with the techniques of microfabrication opens the way to deciphering many cell functions that could not otherwise be elucidated. It represents an important new alliance in research.

The research discussed in this article was supported in part by grants from the National Science Foundation and the Whitehall Foundation.

Hoch



Harvey C. Hoch is an associate professor of plant pathology at Cornell, with headquarters at the New York State Agricultural Experiment Station in Geneva.

Hoch holds the B.S. degree in botany and the M.S. in plant pathology from Colorado State University. He received the Ph.D. in plant pathology from the University of Wisconsin at Madison in 1972. Before joining the Cornell faculty in 1974, he held postdoctoral positions at Wisconsin and at the University of Georgia.

His early research on biological control of fungal-incited diseases emphasized soil microbiology and cytology. For the past eight years he has focused on the cell biology of rust fungi.

Staples

Richard C. Staples is the program director in the area of plant stress at the Boyce Thompson Institute for Plant Research at Cornell.

As an undergraduate, he studied botany and plant pathology at Colorado State University, and in 1957 he received the Ph.D. in plant biochemistry from Columbia University. He has been at the Boyce Thompson Institute ever since, as a fellow in biochemistry, a plant biochemist, and a program director. He came to Cornell in 1977 when the institute opened its laboratory here.

Honors he has received include the Humboldt Senior U.S. Scientist Award, and election as a fellow of the American Phytopathological Society. In 1983 one of his papers was selected as a Citation Classic.

Undergrads on the Research Teams

■ It was an impressive presentation: an afternoon of reports by articulate, knowledgeable Cornell engineering researchers who are still undergraduates. The event, on March 10, was the first Undergraduate Research Forum, the climax of the first full year of the college's innovative Undergraduate Research Involvement Program.

Introducing the speakers was the associate dean for undergraduate programs, Richard N. White (who also took some of the photographs shown here). He was one proud dean. In the front row, and often the first to ask a question, was an alumnus, James Moore '62, who had initiated the project with a $225,000 grant. Among the audience were many of the professors who are supervising the students' research.

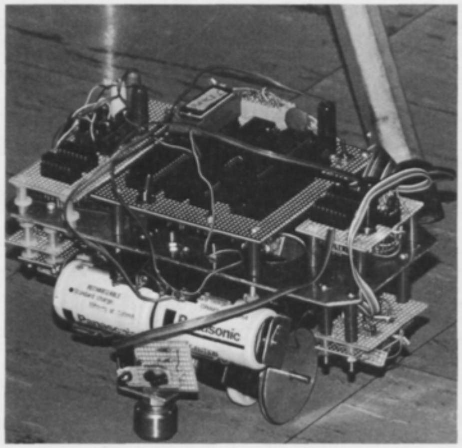
All the participants were interested in everybody else's report: what was accomplished, what was learned, the problems encountered, and sometimes what didn't work out as well as had been hoped. One of the speakers was a Master of Engineering student who had participated last year and got so interested in the project that he decided to continue in graduate school. (He was pinch-hitting for the senior who had succeeded him on the project but was away interviewing for a job.)

The research being reported wasn't ordinary student project work—it was part of ongoing faculty research programs. The wide-ranging topics reflected the breadth and depth of Cornell engineering research; a corporate visitor remarked that this

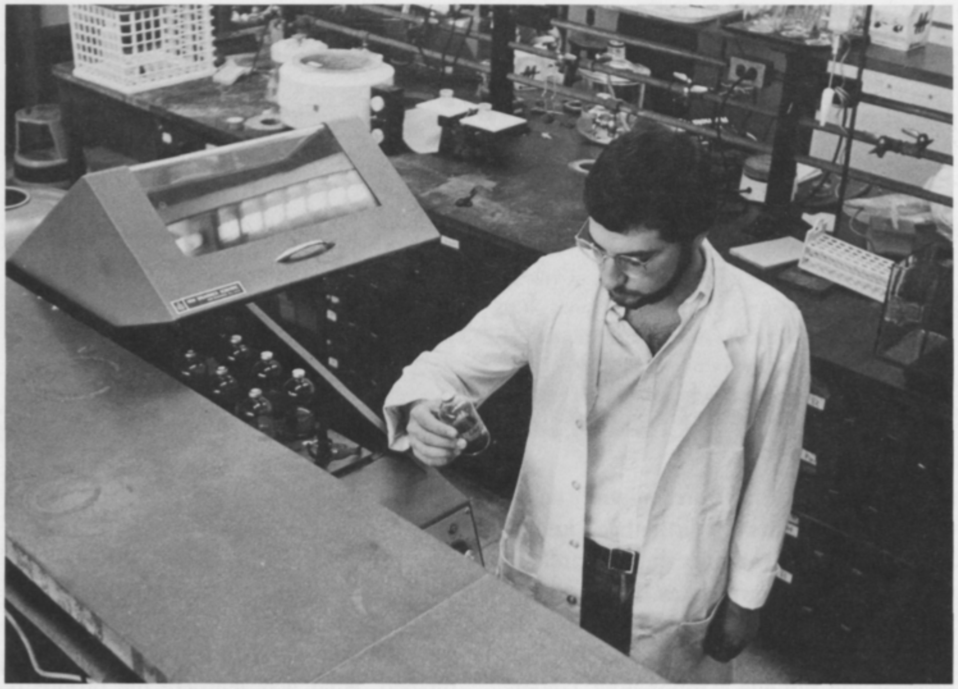
Below: Edward P. Clary, a junior in materials science and engineering, reported on his work with Professor Steven L. Sass. Clary had the opportunity to use a state-of-the-art transmission electron microscope.

Left: A presentation that aroused much interest was Anh Tran's report on facilities at state highway rest areas. Using operations research techniques, she analyzed how needs are being met. One conclusion, which "workers on the scene could have told the planners if there had been better communication," is that there should be a 60:40 rather than a 50:50 ratio of space for women's to men's rest rooms (women take longer). This finding may have repercussions in parks across the country.

Tran gathered data on her summer job last year with the state of Washington; at Cornell she worked with Anthony J. Richardson of the environmental engineering faculty.



Above: The "Roborat" developed by a seven-member student team was demonstrated at the forum. So far its programming enables it to do only "stupid mouse tricks," but in May it is to compete in a national "micromouse" competition in which a maze must be negotiated through the use of sensors and computer memory. Team members, who worked with electrical engineering professor James Thorp, are Chistropher J. Crotty, Valerie Beattie, Steven Chartier, Jeffrey Rothman, Steve Santisi, Henry Tong, and Frank Topolovec.



Right above: Back at the lab, Andrew Lipton showed some of the equipment used in his project (carried out under chemical engineering professors Robert K. Finn and Michael L. Shuler) on an aerobic process for the biodegradation of the carcinogen trichloroethane in groundwater. Samples are incubated and shaken in a controlled environment. Lipton said that one of the main things he has learned so far is to try another way when results are negative.

Right: Saul Fine worked with theoretical and applied mechanics professorAndrew Ruina and postdoctoral associate Jim Papadopoulos on a study of transmission efficiency of bicycles. A linear variable differential transformer (on the floor behind the bicycle) measures voltage as a function of distance traveled. The weights simulate the effect of a rider.

At the break, James Moore talks with Karla Sangrey, a junior in civil engineering.

The students share in the difficulties of planning and executing research, and in the sheer excitement of discovery. They have an opportunity to work closely with faculty members and graduate students, and in doing so they learn that successful research most often comes from a team effort that synthesizes the initiatives of many individuals. They learn to organize themselves for the real world of imperfect answers to somewhat fuzzy questions, and they come to realize that research is not necessarily an esoteric, mysterious process to be undertaken only by geniuses.—Richard N. White

student presentation seemed like a window giving a broad view of research activity at the college.

Usually one student works with one faculty member, but some of the current projects involve as many as seven students. All are upperclass students who earn either academic credit or a stipend. Part of the funding provides for the purchase of equipment, supplies, and computer time. The Moore fund will make $50,000 a year available through 1991.

After the presentation there was a reception, and that evening there was a dinner with the students and their professors as honored guests. In May the students will participate in a research poster session at the annual Cornell Engineering Conference to be held on campus.

Plans for the future are already taking shape. Next year there will be more participants, including underclass students. Overall, the intention is to strengthen the link between teaching and research, and help merge classroom learning and research in the education of Cornell engineers.

Undergraduate Speakers and their Research Topics

Edward P. Clary: *Low Angle Twist Boundaries in Pure* Ni_3Al
Anh Tran: *Rest Area Simulation Modeling*
Gary Boone: *Micromechanical Structures, Biological Analogies, and Nanotechnology*
Jonathan Kohn: *Vibration of Composite Beams*
Hiroyuki Kinoshita: *Polymerization of Thermcon 1000 Monomer by Annealing and Using UV Light*
Emily Chao, Lawrence Davis, and Nancy Wang: *Experimental Investigation of the Biomechanics of the Knee*
Randall Verhoef: *Kinetics of the Oxidation of Hydrogen on Pt(111)*
Karla Sangrey: *Asphalt Concrete Fatigue Behavior*
Andy Rapo and Tejel Gandhi*: *Electrocardiogram Scanning Program*
Miri Park: *Near-Field Optical Lithography*
J. Scott Berg: *GeLi Detector Spectrum Generation Using Monte Carlo Computer Methods*
Soojin Kim: *Interactive Graphical Solutions to 3-D Fluid Flow Problems*
Andrew Lipton: *Aerobic Biodegradation of Trichloroethane*
William McGurk: *Mechanical Implementation of a Rotary Scanning Valve*
Jeffrey Boylan: *Design of a Computer-Controlled Pressure Multiplexer*
David George: *Saving Attributes to Disk Using the Synthesis Generator*
Annie Wang: *Digital Pulse Width Measurer*
Steve Santisi and Valerie Beattie: *Micromouse Project (Electronic Robot)*
Galen Pierce: *Melt Migration in Glass-Ceramic Systems*
Saul Fine: *Transmission Efficiency of Bicycles*
David Briskman (M.Eng.): *Graphical Simulation for Modeling and Analysis*

Computer Science students registered in the College of Arts and Sciences

■ Earlier on the same day as the Undergraduate Research Forum, engineers responded to the architecture students' annual Dragon Day parade around the campus with a knight on horseback (see also the inside back cover).

When the parade passed along the engineering quad—traditionally "enemy territory"—the knight emerged to follow the two-headed dragon. He spared the creature, however, and it met its customary end by fire at the parade's end on the arts quad. Confrontation en route was limited to the launching of a few raw-egg missiles.

The knight on horseback was an innovation this year. During a week of evening sessions, the Phoenix Society (named for last year's flying Mylar phoenix) built a horse that could rear and a rider who could brandish his sword and move his head.

Unlike the dragon, the horse and knight survived, presumably to face the 1989 St. Patrick's Day dragon.

FACULTY PUBLICATIONS

The following publications and conference papers appeared or were presented during the period October through December 1987. (Earlier entries are listed with the year of publication in parentheses.) The names of Cornell personnel are in italics.

■ AGRICULTURAL ENGINEERING

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ENGINEERING
Cornell Quarterly

Published by the College of Engineering
Cornell University

Editor: Gladys McConkey

Associate Editor and Illustrator: David Price

Editorial Assistant: Lindy Costello

Printing: Davis Press
Worcester, Massachusetts

Photography credits:
Charles Harrington: all covers, 1 (1, 2, 4, 5 from top), 2, 4, 5, 7, 8, 14, 23, 29, 38
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Opposite: The engineering students' knight on horseback, who joined this year's Dragon Day parade (see page 38).

ENGINEERING
Cornell Quarterly
(ISSN 0013-7871)
Carpenter Hall, Ithaca, N.Y. 14853

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